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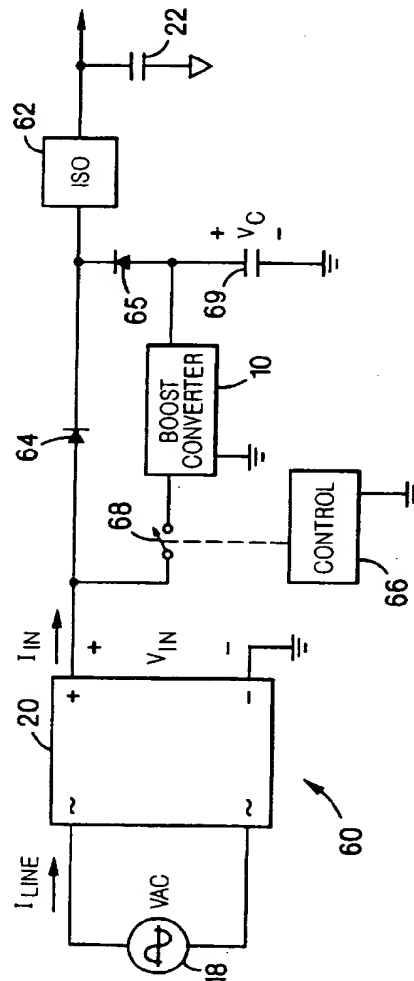
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(54) **Efficient power conversion.**

(57) A power conversion apparatus consisting of boost conversion elements for effecting a boost conversion of power originating from a varying voltage source and additional conversion elements for also effecting conversion of power originating from the varying voltage source is disclosed. Circuitry selectively configures the conversion elements with respect to delivery of power to a load to achieve greater conversion efficiency than if all of the power delivered to the load were constrained to flow through the additional conversion elements and at least some of the boost conversion elements.

Also disclosed is a power conversion scheme in which power is converted from a voltage source having a predetermined source voltage range, and delivered to a load via two sets of power conversion elements. Each set effects conversion of power from the voltage source. At least one of the sets has an input operating voltage range narrower than the source voltage range. The apparatus includes control circuitry for configuring and reconfiguring interconnections of the two sets with the voltage source and the load to provide an input operating voltage range for the apparatus which is greater than the input operating range of the set of power conversion elements having the narrower input operating voltage range.

A way of enhancing the input voltage operating range for a power conversion circuit which has two sets of power conversion elements arranged to share power delivered to a load is also described. The circuit is selectively configured with the two sets in series or not in series in a manner so that the input voltage operating range of the power conversion circuit is broader than the input voltage operating range of either of the sets of power conversion elements.



**FIG. 5**

This invention relates to efficient power conversion.

Typical isolated, power factor corrected, power converters ("IPFC converters") accept power from an AC input voltage source and deliver power to a load at some predetermined value of DC load voltage. They are called "isolated" because they provide a high degree of galvanic isolation between the input voltage source and the load. They are called "power factor corrected" because they control the waveshape and phase of the current drawn by the converter from the AC input source to match the waveshape and phase of the voltage delivered by the AC input source. Unlike non-power factor corrected schemes (found, e.g., in converters which include "capacitive input" rectifiers), power factor correction enables the converter to draw less RMS current for a given value of converter input power. This is useful in allowing a device to withdraw the maximum possible amount of power from an AC branch circuit.

In one known way to implement an IPFC power converter 5 (Figure 1), the bipolar voltage from the AC input source 18, Vac, is delivered to a full-wave rectifier 20. The unipolar, time varying, voltage at the rectifier output, Vin, is delivered to a non-isolated boost converter 10. The boost converter 10 belongs to a class of converters which deliver an output voltage which is greater than the value of the boost converter input voltage, and typically do so for input voltages down to essentially zero volts. PFC controller circuitry 14 delivers a control signal 50 to the boost converter 10 which performs two functions simultaneously. First, it keeps the output voltage, VB, of the boost converter at a predetermined voltage value, Vb, which is (a) above the peak value, Vp, of the rectified voltage Vin and (b) within the input voltage operating range of an isolated DC-DC converter 62. Second, it controls the input current of the boost converter, Iin, to conform to the phase and waveshape of the voltage Vin. The output voltage of the boost converter is filtered and smoothed by a storage capacitor 22 and delivered to the input of an isolated converter 62, which delivers power to the load 23 at a regulated value of output voltage Vo. In general, the isolated converter 62 would include both isolated power conversion circuitry (e.g., a transformer isolated PWM converter; or a transformer isolated zero-current switching converter) and a controller (not shown) for regulating the converter 62 output voltage.

Among the wide variety of known possible implementations of the boost converter and PFC control circuitry is the PWM (pulse-width modulated) boost switching power converter 2 of Figure 2. If the switch 29 is opened and closed at a duty cycle D (where  $D = t_{on}/(t_{on}+t_{off})$ ) then converter 2 will produce an output voltage equal to  $V_{out} = V_{in}/(1-D)$ . Other examples of boost converters and PFC control circuitry are described in our European Patent Application No:

92301978.0 (EP-A-0508595); Wilkerson et al, "Unity Power Factor Supply," U.S. Patent No. 4,677,366; and Williams, "AC to DC Converter With Unity Power Factor," U.S. Patent No. 4,940,929. A complete monolithic PFC controller integrated circuit 14 is sold as Part No. UC1854 by Unitrode Integrated Circuits, Merrimack, N.H., USA.

Among the known possible implementations of the isolated DC-DC converter 62 are various isolated "buck" topologies (e.g., flyback, PWM), zero-current switching "buck" converters (see, for example, Vinciarelli, "Forward Converter Switching at Zero Current," U.S. Patent No. 4,415,959), and resonant converters. In general, a buck converter delivers a voltage to a load which is lower than the value of the converter equivalent input source voltage (which, in typical transformer isolated converters, is the value of the converter DC input voltage reflected into the load side of the transformer--e.g., the converter DC input voltage divided by the transformer turns ratio). An integrated circuit which includes the complete PFC controller 14 and most of the elements of a controller for a PWM DC-DC converter 62 is also available as Part No. UC1891, from Unitrode.

It is known to arrange multiple power converters to share predictably in delivering power to a load. Paralleling of PWM converters in power sharing arrays is described in Unitrode Application Note U-129, "UC3907 Load Share IC Simplifies Parallel Power Supply Design," in the "Unitrode Product & Applications Handbook 1993-94." Power sharing between quantized energy converters (e.g., zero-current switching converters) is described in Vinciarelli, "Power Booster Switching at Zero Current," U. S. Patent No. 4,648,020 (incorporated by reference). Connecting power converter outputs in a fixed series arrangement is shown in Vicor 1991 Product Catalog, Rev. 1, published by Vicor Corporation, Andover, MA 01879, USA.

Power converters are frequently characterized by both a minimum and a maximum value of input operating voltage, Vmin and Vmax. The values of Vmin and Vmax cannot be set arbitrarily because a broader range, the ratio of Vmax to Vmin, comes at the cost of lower conversion efficiency (assuming other factors are equal--e.g., conversion topology, output voltage, converter layout, and size).

Some of the factors which cause this loss in efficiency are illustrated in Figure 3, a partial schematic of an isolated buck converter. A MOSFET switch 11 connected in series with the primary winding of an isolation transformer 15 is turned on and off by a controller 12 to maintain the load 16 voltage at a constant value Vout. The pulsating voltage Vpri and current Isw are reflected into the secondary of the transformer and power is transferred forward to the load 16 via rectifier 18 and output filter 20. The output voltage, Vout, is essentially equal to the average value of the

pulsating voltage,  $V_f$ , delivered to the input of the filter 20. For such a converter, maintaining the load voltage at a value  $V_{out}$  requires that the value of  $V_{in}$  be greater than a value  $V_{min} = N \cdot V_{out}$ . One factor which limits  $V_{max}$  is the maximum voltage rating,  $V_b$ , of the switch 11. Thus, to increase the input operating range, either  $N$ , or  $V_b$ , or both, may be increased. For a MOS-FET switch of a given die size, however, an increase in  $V_b$  results in an increase in switch on-resistance and this will result in increased switch losses. This will be further exacerbated if  $N$  is also increased as a means of decreasing  $V_{min}$ , since, for a given amount of power throughput, lower values of  $V_{in}$  will result in higher average and rms values of  $I_{in}$ . Finally, the turns ratio  $N$  cannot be arbitrarily increased since this will increase both the peak and average values of  $V_f$  when  $V_{in} = V_{max}$  (thereby requiring, for example, a higher voltage, and lossier, rectifier 18) and may also adversely affect the losses and parasitics (e.g., leakage inductance, interwinding and intrawinding capacitances) in the transformer itself.

One way to increase the input operating range of a power converter, while attempting to maintain a given level of efficiency and providing for a given level of power throughput at a given maximum environmental operating temperature, is to make the converter larger (e.g., use more, or larger, components). Thus, in Figure 3, the increased resistance of a higher voltage switch 11 can be partially offset by using more switches in parallel or by using a larger die size switch.

Another way to increase the input operating range of a power converter and satisfy a given maximum operating temperature requirement is simply to accommodate the efficiency loss by reducing the maximum power rating of the converter at maximum operating temperature.

A way to reduce the minimum operating voltage,  $V_{min}$ , of a power converter is to use two converters in a power sharing arrangement with their outputs connected in series. Since, in such an arrangement, each converter need only deliver  $V_{out}/2$  volts to the load, the value of  $V_{min}$  is effectively reduced by a factor of two. Connecting power converter outputs in a fixed series arrangement is shown in the Vicor 1991 Product Catalog, Rev. 1, published by Vicor Corporation, Andover, MA 01879, USA.

In general, in one aspect, the invention features boost conversion elements for effecting a boost conversion of power originating from a varying voltage source; additional conversion elements for also effecting conversion of power originating from the varying voltage source; and circuitry for selectively configuring the conversion elements with respect to delivery of power to a load to achieve greater conversion efficiency than if all of the power delivered to the load were constrained to flow through the additional conversion elements and at least some of the boost con-

version elements.

Practical implementations may include the following features. The circuitry may selectively configure the conversion elements so that during some periods the power delivered to the load is constrained not to flow through the boost conversion elements. The power may be constrained not to flow through the boost conversion elements more than half of the time. The circuitry selectively may configure the conversion elements based on the voltage level of the varying voltage source, e.g., when the voltage level of the varying voltage source falls within a specific range of values. The circuitry may selectively configure the conversion elements based on when the voltage level of the varying voltage source passes a threshold, e.g., a threshold based on a minimum input operating voltage of the additional conversion elements.

The power converted by the boost conversion elements may be delivered to the additional conversion elements for conversion. All of the power converted by the boost conversion elements may be delivered to the additional conversion elements for conversion, e.g., delivered via a unidirectional element biased to permit current to pass only from the boost conversion elements toward the additional conversion elements. Or the power converted by the boost conversion elements may be delivered via a short circuit path directly to the additional conversion elements. During the periods when the power is constrained not to flow through the boost conversion elements, it may be delivered from the voltage source to the additional conversion elements via a unidirectional component. The voltage source may be connected to the boost conversion elements via a switch which in one state disconnects the voltage source from the boost conversion elements. The voltage source may be connected to the boost conversion elements via a short circuit path. The circuitry for selectively configuring the conversion elements may include a switch controller for controlling the switch. The additional conversion elements may have a minimum input operating voltage and the boost conversion elements may deliver power to the additional conversion elements at a voltage which is greater than the minimum input operating voltage of the additional conversion elements.

The additional conversion elements may provide galvanic isolation between the source and the load. A power factor correcting controller may be used to cause variations in current drawn from the voltage source to follow variations in voltage of the voltage source. The power factor correcting controller may be associated with the additional conversion elements. The power factor correcting controller may regulate the voltage across the load to a predetermined value.

The voltage source may include an AC source and there may be a full wave rectifier for rectifying the AC source. The rectified power from the input

power source may be delivered via a short circuit path directly to the input of the boost conversion elements.

The additional conversion elements may include a pair of converters operating in a power sharing arrangement. Reconfiguration control circuitry may connect the pair of converters either in series or in parallel. The power sharing arrangement may include power sharing control circuitry. The reconfiguration control circuitry may connect the pair of converters in series (or in parallel) when the voltage of the input source crosses a threshold. The threshold may be related to the maximum input operating voltage of either converter. The converters may share essentially equally in the power delivered to the load. The converters may include ZCS converters. One of the ZCS converters may include a booster and the other ZCS converter may include a driver.

Each of the converters of the pair may have a positive input and a negative input, and a switch may connect the positive inputs of the two converters, a switch may connect the negative inputs of the two converters, and a diode may connect the positive input of one of the converters to the negative input of the other converter. There may be output control circuitry for connecting the outputs of the pair of converters either in series or in parallel, e.g., connecting the outputs of the pair of converters in series (parallel) when the voltage at the input of the converters crosses a threshold. The threshold may be based upon the minimum input operating voltage of either converter.

There may be separate full wave rectifier circuits, the first rectifier circuit being interposed between the input source and the boost conversion elements, and the second rectifier circuit being interposed between the input source and the additional conversion elements. The output of the second rectifier circuit may be connected by a short circuit path to the input of the additional conversion elements. The rectifier circuits may include six unidirectional elements forming two bridges each having four of the unidirectional elements, two of the unidirectional elements belonging to both bridges, one of the bridges having its output connected to the boost conversion elements, the other having its output connected to the additional conversion elements.

In general, in another aspect, the invention features a method for converting power from a varying voltage source and delivering it to a load, by causing selectively (a) a boost conversion of power originating from the varying voltage source in boost conversion elements, and (b) another conversion of power originating from the varying voltage source in additional conversion elements; in a manner, with respect to delivery of power to the load, to achieve greater conversion efficiency than if all of the power delivered to the load were constrained to flow through the additional conversion elements and at least some of the boost

conversion elements.

Practical implementations may include the following features: The conversions may be caused selectively to achieve a greater input voltage operating range for the apparatus than if all of the power delivered to the load were constrained to flow only through the additional conversion elements. The inputs (outputs) of the two converters may be connected in parallel or series.

In general, in another aspect the invention features apparatus for converting power from a voltage source having a predetermined source voltage range, and delivering it to a load via two sets of power conversion elements, each set for effecting conversion of power from the voltage source, at least one of the sets having an input operating voltage range narrower than the source voltage range. The apparatus includes control circuitry for configuring and reconfiguring interconnections of the two sets with the voltage source and the load to provide an input operating voltage range for the apparatus which is greater than the input operating range of the set of power conversion elements having the narrower input operating voltage range.

In general, in another aspect, the invention features a method for enhancing the input voltage operating range of a power conversion circuit which has two sets of power conversion elements arranged to share power delivered to a load. The method includes selectively configuring the circuit with the two sets in series or not in series in a manner so that the input voltage operating range of the power conversion circuit is broader than the input voltage operating range of either of the sets of power conversion elements.

Among the advantages shown by practical embodiments described hereinbelow are that power conversion is enabled with greater efficiency while providing power correction and isolation.

The invention is hereinafter more particularly described by way of example only with reference to the accompanying drawings, in which:-

Figure 1 is a circuit diagram of an IPFC power converter including a boost converter;

Figure 2 is a circuit diagram of a portion of a non-isolated boost converter;

Figure 3 is a circuit diagram of a portion of a buck converter;

Figure 4 is a circuit diagram of an isolated converter with a power factor correcting controller;

Figure 5 is a circuit diagram of a quasi-single stage IPFC converter constructed in accordance with the present invention;

Figure 6 shows waveforms for input voltage, input current and input power for the converter of Fig. 5;

Figure 7 is a schematic diagram of an alternative converter arrangement, also constructed in accordance with the present invention;

Figure 8 is a diagram of a circuit for selectively connecting the inputs of two power converters either in series or in parallel in an embodiment of a system in accordance with the present invention;

Figure 9 is a circuit diagram of another quasi-single stage IPFC converter, also constructed in accordance with the present invention;

Figure 10 is a circuit diagram modelling a portion of the converter of Figure 9;

Figure 11 is a circuit diagram of a quasi-single stage IPFC power converter, also constructed in accordance with the present invention.

Figure 12 is a circuit diagram showing additional details of a portion of the circuit of Figure 11;

Figure 13 shows waveforms for the converter of Figure 12;

Figure 14 is a diagram of a circuit for selectively connecting the outputs of a pair of converters in series or in parallel in an embodiment of a system in accordance with the present invention; and

Figure 15 is a circuit diagram of another power converter constructed in accordance with the present invention.

In the IPFC converter 5 of Figure 1 the boost converter serves two essential functions throughout the entire AC source voltage cycle. First, it presents a power factor corrected load to the AC source. Second, it maintains the voltage  $V_B$  at a level above both the minimum operating voltage,  $V_{min}$ , of the DC-DC converter 62 and the peak value,  $V_p$ , of the AC source 18 over the specified AC input voltage operating range of the converter 5. Because all of the power drawn by the DC-DC converter 62 is delivered via the boost converter 10, i.e., a two-stage approach, the overall conversion efficiency of the converter 5 is the product of the conversion efficiencies of the two power conversion stages 10, 62. Thus, if the boost converter 10 and the isolated converter 62 have respective conversion efficiencies of 90% and 85%, then the overall conversion efficiency of the complete converter 10 will be  $0.90 \times 0.85 = .765$ , or 76.5%.

The features provided by the boost converter in Figure 1 are needed only during the portion of the AC operating cycle when the voltage  $V_{in}$  is below the minimum operating voltage,  $V_{min}$ , of the isolated converter 62. If the boost converter were eliminated and the PFC controlled the isolated converter 62 operating by itself (as shown in Figure 4), then the isolated converter 62 could perform both output voltage regulation and power factor correction throughout those portions of the cycle that  $V_{in}$  is above the minimum input operating voltage,  $V_{min}$ . These time periods are labeled Top in the waveform in Figure 4. But during the remainder of the cycle, when  $V_{in}$  is below  $V_{min}$ , the isolated converter would no longer be able to reliably regulate the voltage  $V_{out}$  or to control the phase and waveshape of the current  $i_{in}$ . This would cause

distortions in the output voltage,  $V_{out}$ , and the input current,  $i_{in}$ , and result in degraded power factor correction performance. The degree of performance degradation would even vary with changes in the value of the AC line voltage (e.g., the voltage  $V_p$ ) because those changes would affect the relative amounts of time that the converter 62 was operational and non-operational during an AC line cycle.

The inclusion of boost converter 10 overcomes these problems by maintaining the converter input voltage above  $V_{min}$ . But operating the boost converter throughout the entire AC line cycle has a significant drawback: because both the input voltage and current are sinusoidal and in phase, the majority of power is drawn from the line at or near the peak of the AC line cycle, and it is under these operating conditions that the boost converter will exhibit the greatest portion of its overall power loss. Yet, the benefit of the boost converter is needed only when the line voltage is low, e.g., below  $V_{min}$ , not when the line is near its peak value. Thus, the boost converter produces its greatest negative impact on overall converter efficiency during the time period when it is not actually needed—during the time period when the AC source voltage is above  $V_{min}$ .

As shown in Figure 5, in a quasi-single stage, IPFC converter circuit 60 a boost converter 10 delivers power to an isolated converter 62 for only a portion of an AC line cycle. The isolated converter 62 may be any isolated converter having a minimum operating voltage  $V_{min}$  and the boost converter 10 may be any non-isolated boost converter. Isolated converter 62 includes a power factor correction controller (not shown, but which may be any of the controllers previously mentioned) which controls the current  $i_{in}$  to follow the waveshape of  $V_{in}$  and which also controls the output voltage of the converter 62 to be regulated at a predetermined value  $V_{out}$ . The boost converter is arranged to maintain its output voltage,  $V_c$ , at a predetermined value which is at, or slightly above, the minimum input operating voltage of the isolated converter 62. Full wave rectifier 20 converts the bipolar AC source voltage  $V_{ac}$  18 into a unipolar voltage  $V_{in}$ . Switch control circuitry 66 closes switch 68 whenever the rectified line voltage,  $V_{in}$ , is below an activation threshold value which is also set to be above the minimum operating voltage of the isolated converter 62. When the switch 68 is closed, the boost converter is activated and supplies current to the isolated converter input, via diode 65, thereby maintaining the input voltage to the isolated converter 62 above its minimum operating voltage  $V_{min}$ . During the time that the boost converter 10 is supplying power to the isolated converter 62, the power factor correction controller in the isolated converter continues to force the current  $i_{in}$  to follow the waveform of the voltage  $V_{in}$  (and therefore forces the bipolar AC line current  $i_{line}$  to follow the waveform of the AC source voltage  $V_{ac}$ ). Ca-

capacitor 69 accepts the time varying current delivered by the boost converter and minimizes time variations in the voltage  $V_c$ . Since  $V_{in}$  is less than  $V_c$  during this period, diode 64 is reverse biased and the overall converter 60 operates in a "two-stage" mode with all of the power drawn by the isolated converter 62 being supplied by the boost converter 10.

When the voltage  $V_{in}$  rises above the activation threshold the switch is opened by control circuitry 66 and the boost converter ceases operating. Power is delivered directly from the full-wave rectifier 20 to the isolated converter via diode 64. Since the value of  $V_c$  is below  $V_{in}$  during this time, diode 65 is reverse biased. During the time that the switch 68 is open the power factor correction controller in the isolated converter causes the converter 62 to appear as a power factor corrected load to the AC source 18 and also controls the converter 62 to regulate the output voltage of the converter 62 at a value  $V_{out}$ . Output capacitor 22 stores energy as the input AC line voltage, and consequently both the input current and power output of the isolated converter fluctuate in time under the control of the power factor correction controller included in the converter 62. The capacitor charges during times of high power output from the converter 62 (e.g., when the voltage  $V_{in}$ , and current  $I_{in}$ , are relatively high) and discharges when the power output from the converter is low (e.g., when  $V_{in}$  and  $I_{in}$  are relatively low).

The power conversion topology shown in Figure 5 is "quasi-single stage", since the switch is closed for "two-stage" operation for only a small fraction of each energy cycle. At all other times during the energy cycle, energy is processed only by the isolated converter 62. This can substantially improve the overall conversion efficiency as compared to the converter 5 of Figure 4.

For example, assume the following. Both the minimum operating voltage of the isolated converter 62,  $V_{min}$ , and the switch 68 activation threshold are 50 Volts. The AC line voltage is 85 VAC (for which  $V_p = 120$  V). The efficiency of the boost converter is 90% and the efficiency of the isolated converter is 85%. And the converter 60 is delivering power to a load and drawing 500 Watts from a sinusoidal AC source 18.

Under those assumptions, both the input voltage,  $V_{in}$ , and the input current,  $I_{in}$ , (Figure 6) will be unipolar sinusoids (due to the action of the rectifier and the power factor correcting controller in the isolated converters 62) and the peak value of  $I_{in}$  will be 8.31 Amperes. The input power, which is the product of  $V_{in}$  and  $I_{in}$ , will peak at 1000 Watts. During the shaded portions of the waveforms, when the voltage  $V_{in}$  is below  $V_{min}$ , the power is processed by both converters 10, 62. In the example, the power processed during this time is only 3.2% of the total power, or 16.1 Watts. The remainder of the power, 483.9 Watts, is processed during the balance of the AC line cycle and this

power processing is done solely by the isolated converter 62. As a result, the power loss during the shaded portion of the cycle, when both converters are processing power, is

$$5 \quad 16.1 * (1 - 0.90 * 0.85) = 3.78 \text{ Watts,}$$

and the power loss during the balance of the cycle, when only the isolated converter 62 is processing power, is

$$10 \quad (1 - 0.85) * 494.4 = 74.16 \text{ Watts,}$$

resulting in a total loss of 77.94 Watts. Since the power delivered to the load is  $500 - 3.78 - 77.94 = 418.28$  Watts, the overall efficiency of the converter 60 is  $418.28 / 500 = 0.837$ , or 83.7%. This is not much worse than the efficiency of the isolated converter 62 alone and is significantly better than the 76.5% efficiency exhibited by the converter 10 of Figure 1 in which both converters 10, 62 continuously process power throughout the entire AC line cycle.

An alternative implementation of a quasi-single stage converter eliminates switch 68, switch controller circuitry 66, and diode 64 (Figure 5). The boost converter 10 in Figure 7 includes the circuit components of the boost converter of Figure 2, although, in general, any non-isolated boost topology could be used. In operation, the voltage controller 26 in the boost converter maintains the voltage  $V_c$  at a predetermined value,  $V_t$ , which is above the minimum operating voltage of the converter 62. When the voltage  $V_{in}$  is below  $V_t$ , the IPFC converter 61 will operate in essentially the same way as the IPFC converter 60 of Figure 5. When  $V_{in}$  is above  $V_t$ , however, the voltage controller 26 will force the duty cycle of the switch 28 to be zero and the switch 28 will be off. With the switch 28 off, the voltage  $V_{in}$  will be impressed across the series circuit comprising the capacitor 69 and the diode 64. If the value of the capacitor 69 were large, connection of this circuit across  $V_{in}$  could substantially impact the power factor which the converter 61 presents to the AC line. Because the amount of power processed by the boost converter 10 is small, however, so too is the value of the capacitor 69.

For example, in a practical converter 60 of the kind shown in Figures 5 and 7, designed to deliver up to 750 Watts to a load, the value of capacitor 69 is 1 microfarad (for comparison, in a practical implementation of a converter of the kind shown in Figure 1, designed to operate at the same power level, several hundred microfarads of filter capacitor 22 would typically be required). For a converter of the kind shown in Figure 7, impressing  $V_c$  across this small value of capacitance has only a minor impact on the power factor that the IPFC converter 61 presents to the AC source 18.

A benefit of the topology of Figure 5 is that the components in the boost converter 10 need only withstand the relatively low voltages which are present when the switch 68 is closed. As  $V_{in}$  rises, and the switch opens, the combination of the switch 68 and

the diode 65 protect the components in the boost converter 10 from elevated values of  $V_{in}$ . The boost converter may then be smaller and use less costly components. And semiconductor switches (e.g., power MOSFETs) having lower voltage ratings may be used, which improves conversion efficiency. Another benefit is that boost converters operating at low power and low voltage can be designed to operate at higher operating frequencies, also allowing smaller components. Also, in contrast to the topology of Figure 7, the capacitor 69 of Figure 5 is never passively connected across  $V_{in}$  and so will not affect power factor when the boost converter is not operating.

In other implementations of the IPFC converter of Figure 5, switch 68 and switch controller 66 are included but the diode 65 is omitted and replaced with a short circuit. The effect of the capacitor 69 on power factor then will be essentially the same as in the converter 61 of Figure 7, but the combined effect of the switch 68 and the output diode in the boost converter (e.g., diode 34, Figure 2) will protect the majority of components in the boost converter 10 (e.g., in Figure 7, switch 28, controller 26) from high values of  $V_{in}$ .

Embodiments of the boost converter 10 used in the IPFC converter 60 of Figure 5 (as well as in all of the IPFC converter embodiments described herein) must maintain the voltage  $V_c$  at or above the minimum operating voltage of the isolated converter 62 while their input current is being controlled (by the PFC controller in the isolated converter 62) to follow the waveform of the line voltage. This requires that both the energy storage elements in the boost converter be relatively small and that the bandwidth of the converter be much greater than the AC source frequency. For example, with reference to Figures 2 and 5, a PWM boost converter was constructed for use in an IPFC converter designed to deliver 750 Watts to a load while operating over an AC line voltage range of 85 V, rms, to 264 V, rms (50 or 60 Hz line frequency). The activation threshold of the switch 68 (Fig. 5) was in the range of 50 to 70 Volts. The switch 68 was an IRF840 MOSFET, having a breakdown voltage rating of 500 V, manufactured by International Rectifier Corporation, El Segundo, Ca., USA. The value of inductor 32 (Fig. 2) was 60 microhenries. The value of the boost converter output capacitor 69 was 1 microfarad. The output diode 34 in the boost converter was a 50SQ100 Schottky diode and the boost converter switch 28 was an IRF540 MOSFET, each having a breakdown voltage rating of 100 V and each manufactured by International Rectifier. An integrated circuit controller, part number UC3842, manufactured by Unitrode, was used to control the boost converter at a switching frequency of approximately 150 KHZ. Diode 65 (Fig. 5) was a 1N5406 rectifier, manufactured by Motorola, Inc., Phoenix, AZ USA.

In many applications it is desirable for an IPFC converter to operate over a relatively wide range of

AC input voltages, for example over a range from 85 VAC, rms to 264 VAC, rms (corresponding to a range of peak values of  $V_{ac}$  and  $V_{in}$  of 120 Volts to 373 Volts). This would require that the isolated converter 62 be able to operate at input voltages approaching 400 Volts, DC. If the minimum input operating voltage of the isolated converter were 50 Volts, then the converter would have to have an 8:1 range of input operating voltage. As a practical matter, both the operating efficiency and power density of typical isolated converters degrade as the input operating voltage range increases. In general, then, it is desirable to minimize the operating voltage range of the converter 62.

In Figure 8, isolated converters 62, 70 may be used to operate over a range of variation of converter input voltage  $V_{in}$  33 which is greater than the input operating range of the converters themselves. The outputs of two isolated converters 62, 70 are connected in parallel, and made to share in delivering current to the load 23,  $I_{load}$ , by current sharing circuitry 100. For example, if the converters 62, 70 include power conversion circuitry of the kind which deliver power by means of quantized energy transfer, then current sharing may be achieved by connecting the converters in any of the master-booster arrangements described in Vinciarelli, "Power Booster Switching at Zero Current," U.S. Patent No. 4,648,020 (incorporated by reference). Thus, converter 70 may be a driver module, and converter 62 a booster module. The booster module may be operated synchronously and in phase with the driver module (in which case the current sharing controller would simply be circuitry which carries operating frequency information from driver module 70 to booster module 62; see, for example, Figure 12). Or the booster module may be synchronized with a phase delay to reduce conducted noise reflected from the converter inputs back towards the AC source. In either case, the natural power sharing characteristic of zero-current switching converters (and other kinds of quantized power converters) will cause the current delivered by each converter,  $I_{o1}$  and  $I_{o2}$ , to be a predictable fraction of the total amount of current,  $I_{load}$ , delivered to the load 23.

If converters 62, 70 share equally in delivering power to a load, they will also draw essentially equal amounts of power at their inputs. If the inputs to the converters 62, 70 are connected in series across an input source, the average voltages across the inputs of the two converters will be essentially the same.

Switches 76, 78 alternate the inputs of the isolated converters between series and parallel connection. Assume, for example, that each converter 62, 70 has an input operating range of 50 V to 200 V (a 4:1 range). When  $V_{in}$  is below a reconfiguration threshold of between 180 and 200 V, switches 76, 78 are closed by reconfiguration controller 112. Diode 80 connecting the isolated converters is reverse biased. The in-



puts to the isolated converters are thus in parallel, and the input voltages 82, 84 to the two isolated converters are the same and equal to  $V_{in}$ .

When the input voltage  $V_{in}$  33 is above the reconfiguration threshold voltage, switches 76, 78 are opened by the reconfiguration controller 112, thereby connecting the inputs of the two isolated converters 62, 70 in series with each other and with diode 80. Since  $V_{in}$  divides essentially equally across the inputs of the two converters, the series connection of the isolated converters allows increasing the value of  $V_{in}$  to a value which is twice the maximum rated input voltage of the converters 62, 70. Then a pair of converters having a minimum input operating voltage of 50 V and a maximum input operating voltage of 200 V (a 4:1 input voltage range) can be used to handle values of  $V_{in}$  up to 400 V. Thus the total effective input operating range has been increased to 8:1, or double the range of either of two converters 62, 70 taken alone.

The technique of Figure 8 may be used in the quasi-single stage topology of Figure 5 to allow use of isolated converters having an input operating range which is reduced relative to the range of variation of the AC source voltage. The modified circuit 60', shown in Figure 9, has two isolated converters 62, 70 each having a 50-200 V input (4:1) range. A boost converter 10, activated by switch 68 via control circuitry 66, maintains a 50 V output at node 33 when the input voltage,  $V_{in}$ , is below 50 V. The output of the boost converter is fed to the input of the isolated converters 62, 70 via a diode 72 which disconnects the boost converter 10, and capacitor 96, from  $V_{in}$  when the input voltage  $V_{in}$  is above 50 V peak.

Capacitor 22 stores energy as the power factor corrected input current  $I_{in}$ , and the converter output currents,  $I_{o1}$  and  $I_{o2}$ , fluctuate during each line cycle. The capacitor 22 charges during times of high converter 62, 70 power output and discharges when the power outputs are low, thus minimizing fluctuations in the voltage across the load 23.

Reconfiguration controller 112 measures  $V_{in}$  and controls the opening and closing of switches 76, 78 to alternate the inputs of the isolated converters 62, 70 between a series and parallel connection, as described above. Thus, converters having a minimum input operating voltage of 50 V and a maximum input operating voltage of 200 V (a 4:1 input range) can be used in an IPFC converter 60' capable of handling lines having peak voltages up to 400 V (e.g., an AC source voltage 18,  $V_{ac}$ , of up to 282 VAC, rms).

One issue in series-connecting the converters 62, 70 is illustrated in Figure 10. Each converter module is represented by a switching element 94, 96 in series with a load. The switching elements are representative of switches which are typically included in the power conversion circuitry in such a converter and which are opened and closed at switching fre-

quencies much greater than the frequency of the AC source (e.g., source 18, Figure 9). If the switching elements 94, 96 are opened and closed at different points in time the voltage  $V_{in}$  could divide unevenly across the inputs of the two converters (on a transient basis) which might overstress the unit exposed to the higher voltage. To prevent this, a small capacitor (e.g., 0.1 microfarads) may need to be placed across the inputs of each converter 62, 70 to smooth the voltage during any such transient condition.

In Figure 11, reconfiguration controller 112 alternates the inputs of the isolated converters 62, 70 between series and parallel connection, when the line input voltage 18 has a magnitude above and below 180 V, respectively. The reconfiguration controller 112 has a comparator 102 with inputs from a voltage divider composed of resistors 103, 104 and a reference voltage 105. Resistor 37 introduces hysteresis into the controller 112 to reduce the possibility of noise causing spurious switching of the comparator 102. The output of the comparator is a signal that can assume a high or a low value.

Resistors 103, 104 are chosen so that when the input voltage 18 is at 180 V, the voltage at input 106 of the comparator is slightly larger than the reference voltage 105, and the output voltage of the comparator is at its high value. This high value is delivered to inverting switch drivers 108, 110, opening MOSFET switches 76, 78 and placing the isolated converter inputs in series, as required.

Similarly, when  $V_{in}$  is below 180 V, resistors 103, 104 provide a voltage lower than the reference voltage 105, so that the output of comparator 102 changes to its low value. The inverting switch drivers 108, 110 then switch their outputs to their high value, which closes switches 76, 78, placing the inputs of isolated converters 62, 70 in parallel.

In Figure 11 the boost converter 10 is connected to the AC source differently than in Figure 5, where a single full wave rectifier 20 supplies rectified line voltage ( $V_{in}$ ) to the boost converter. The Figure 5 scheme requires diode 64 to isolate the boost converter output voltage,  $V_c$ , from  $V_{in}$  during the time that  $V_{in}$  is below  $V_c$ . As  $V_{in}$  rises and the boost converter ceases operating, all of the current delivered from the AC source to the isolated converter 62 must flow through three diodes: two diodes in the full-wave rectifier 20 and diode 64. This occurs when the current  $I_{in}$  is relatively high, so the presence of diode 64 will cause unnecessary losses. In Figure 11, two additional diodes 220, 222 are added which, in combination with diodes 120, 126 act as a full wave rectifier at the input to the boost converter. With the additional two diodes 220, 222 shown in Figure 11, diodes 122, 118 in the full wave rectifier of Figure 11 will perform the function of the diode 64 in Figure 5--isolating the boost converter input and output when the absolute value of  $V_{ac}$  is below the voltage delivered by the



One way to implement power sharing circuitry 100 is shown in Figure 12. In the Figure, which shows a portion of the converter 60' of Figure 11, the MOS-FET switching element 850 in the isolated driver module 70 is shown being driven by a pulse train delivered by ZCS controller 802. This pulse train, which pulsates between a low value of essentially zero volts and a high value of between 10 and 15 volts, is the frequency signal 806 which is delivered, via current limiting resistor 821, to the light emitting diode 825 at

Efficiency can be further improved by alternating the outputs of the two isolated power converters be-

tween a series and parallel connection. The series connection compensates for the fact that below a certain input voltage threshold, each isolated converter is unable to maintain the desired output voltage. In theory, an isolated buck converter with an internal isolation transformer having a primary-to-secondary turns ratio  $N$  is limited to delivering an average output voltage  $V_o$  only when its input voltage is above  $N \cdot V_o$ . Thus, for example, an isolated converter producing an output voltage of 5 VDC, and having an isolation transformer with a turns ratio  $N = 10$ , will not be able to maintain its output voltage in regulation if the converter input drops below 50 V.

A way to deliver 5 V when the input voltage drops below 50 V is shown in Figure 14. In IPFC converter 360 (only a portion of which is shown), a switch 250 and two diodes 262, 264, provide for connecting the outputs of two isolated converters 62, 70 either in series or in parallel. When switch 250 is closed the outputs of the isolated converters are connected in series and each isolated converter need only deliver 2.5 V at its output to maintain the total output voltage at 5V. Each isolated converter can continue to maintain a 2.5 V output down to a 25 V input, so that the input operating range of the pair of converters 62, 70 is effectively doubled. When the switch 250 is opened, the converter outputs are paralleled via diodes 262, 264.

Figure 14 also shows how the output switching technique may be incorporated into the IPFC converter of Figure 11. An output switch controller 113 is added (in addition to the reconfiguration controller 112). A resistive divider (resistor 259 in series with the resistor string used by the reconfiguration controller 112) and a reference voltage source 256, indicative of a voltage,  $V_x$ , slightly above the minimum input operating voltage of the converters 62, 70, are fed into comparator 252. As  $V_{in}$  drops below  $V_x$  the comparator output signal 258 changes to a state which turns switch 250 on. Because the output switch controller 113 and the switch 250 are on different sides of the isolation barrier, the comparator output signal 258 is delivered to the switch 250 by a galvanically isolated driver 260 (e.g., an opto-coupler).

If both output switching (via output switch controller 113) and input switching (via reconfiguration controller 112) are used in an IPFC converter 360, the overall improvement in equivalent input operating range may be as great as a factor of 4. For example, if the converters have a 4:1 input operating the equivalent input operating range is increased to 16:1. An IPFC converter 360 using converters 62, 70 having minimum and maximum input voltage ratings of 50 V and 200 V, respectively, will be able to operate at values of  $V_{in}$  between 25 V and 400 V, corresponding to AC line voltages between 17.7 VAC, rms and 283 VAC, rms. Another benefit of reducing the equivalent input operating voltage is that the boost converter 10 operating threshold may be lowered by almost a fac-

tor of two (e.g., to around 25 V), further reducing the amount of power processed by the boost converter 10 and further improving the overall efficiency of the IPFC converter 360.

Because selectively connecting converter inputs and outputs in series and parallel increases both input operating voltage range and operating efficiency, it is a fruitful approach in a wide variety of applications. The scheme is not limited to a pair of converters; the number of converters connected in series may be increased indefinitely to extend the upper threshold of the power conversion to any desired value. In the example of Figure 15, a power conversion circuit 399 has at least four converters 400, 402, 404, 406 each characterized by a minimum input operating voltage,  $y$ , and a maximum input operating voltage  $x$  (and an input operating range of  $x:y$ ). For values of input voltage,  $V_{in}$  407, between  $x$  and  $y$ , the inputs of the converters are connected in parallel by closing switches 410 through 420 in the circuit. When the input voltage approaches the maximum input operating voltage,  $x$ , switches 410, 412 are opened, connecting the parallel pair of converters 400, 402 in series with the parallel pair 404, 406. As explained above in connection with Figure 11, the maximum input operating voltage is thus doubled to  $2x$ . Similarly, as  $V_{in}$  approaches a value  $2x$ , switches 414, 416, 418, 420 are opened, connecting the inputs of all four converters in series and increasing the maximum input operating voltage to  $4x$ . Thus, a series connection of  $2n$  converters may be used to provide a maximum input operating voltage of  $2nx$ . A controller for switches 410 through 420 is a simple extension of the reconfiguration controller 112.

Switching the outputs of two converters from a series to a parallel connection may also be extended to any number of power converters (e.g.,  $2n$ ) to decrease the lower threshold  $y$  of the conversion circuit to  $y/2n$ . For example, as shown in Figure 15, when the input voltage 407 is above  $y$  volts the outputs of all of the converters 400, 402, 404, 406 are connected in parallel via diodes 600 through 612. As  $V_{in}$  declines toward  $y$  volts, switch 502 is closed connecting the paralleled outputs of the pair of converters 400, 402 in series with the paralleled outputs of the pair of converters 404, 406. Then each converter need only deliver  $V_{out}/2$  volts (neglecting voltage drops in diodes and switches) to maintain a total converter 399 output of  $V_{out}$ , and, as discussed above, this reduces the minimum operating voltage of the converter 399 to  $y/2$ . If the input voltage further decreases below  $y/2$  volts, switches 508, 510 are thrown so that the outputs of all four converters are in series. Each converter need now only deliver  $V_{out}/4$  volts, which extends the minimum input operating voltage down to  $y/4$  volts. If the output of  $2n$  converters are connected in series, the power conversion circuit can continue to product an output of  $V_{out}$  volts down to an input vol-

tage of  $y/2n$ .

A switch controller for the converter outputs is a simple extension of the dual output switch converter 113.

Other embodiments are feasible. For example, the isolated converters may be of any converter topology (e.g., PWM, resonant); and any of the converters may be isolated or non-isolated.

## Claims

1. Apparatus for converting power from a varying voltage source and delivering it to a load, comprising boost conversion elements adapted for operatively effecting a boost conversion of power originating from the varying voltage source, characterized in further comprising: additional conversion elements also adapted for operatively effecting conversion of power originating from the varying voltage source; and circuitry adapted for operatively selectively configuring the conversion elements with respect to delivery of power to the load to achieve greater conversion efficiency than if all of the power delivered to the load were constrained to flow through the additional conversion elements and at least some of the boost conversion elements.
2. Apparatus according to Claim 1, further characterized in that the circuitry is arranged to selectively configure the conversion elements so that during some periods, preferably for more than half of the time, the power delivered to the load is constrained not to flow through the boost conversion elements.
3. Apparatus according to Claims 1 or 2, further characterized in that the circuitry is arranged to selectively configure the conversion elements based on the voltage level of the varying voltage source.
4. Apparatus according to Claims 1 or 2, further characterized in that the circuitry is arranged to selectively configure the conversion elements based on when the voltage level of the varying voltage source falls within a specific range of values.
5. Apparatus according to Claims 1 or 2, further characterized in that the circuitry is arranged to selectively configure the conversion elements based on when the voltage level of the varying voltage source passes a threshold.
6. Apparatus according to Claim 5, further characterized in that the threshold is based on a mini-

mum input operating voltage of the additional conversion elements.

7. Apparatus according to any preceding claim, further characterized in that power converted by the boost conversion elements, preferably all such power, is operatively delivered to the additional conversion elements for further conversion.
8. Apparatus according to Claim 7, further characterized in that power converted by the boost conversion elements is operatively delivered to the additional conversion elements via a unidirectional element biased to permit current to pass only from the boost conversion elements toward the additional conversion elements.
9. Apparatus according to Claim 7, further characterized in that power converted by the boost conversion elements is operatively delivered via a short circuit path directly to the additional conversion elements.
10. Apparatus according to Claim 2 or any claim appendant thereto, further characterized in that during the periods when the power is constrained not to flow through the boost conversion elements, it is operatively delivered from the voltage source to the additional conversion elements via a unidirectional component.
11. Apparatus according to any preceding claim, further characterized in that the voltage source is connected to the boost conversion elements via a switch which in one state disconnects the voltage source from the boost conversion elements.
12. Apparatus according to Claim 11, further characterized in that the circuitry adapted for operatively selectively configuring the conversion elements comprises a switch controller for controlling the switch.
13. Apparatus according to any of Claims 1 to 10, further characterized in that the voltage source is connected to the boost conversion elements via a short circuit path.
14. Apparatus according to any preceding claim, further characterized in that the additional conversion elements have a minimum input operating voltage and the boost conversion elements are adapted to deliver power to the additional conversion elements at a voltage which is greater than the minimum input operating voltage of the additional conversion elements.
15. Apparatus according to any preceding claim, fur-

ther characterized in that the additional conversion elements operatively provide galvanic isolation between the source and the load.

16. Apparatus according to any preceding claim, characterized in further comprising a power factor correcting controller, preferably associated with the additional conversion elements which is arranged operatively to cause variations in current drawn from the voltage source to follow variations in voltage of the voltage source. 5 10
17. Apparatus according to Claim 16, further characterized in that the power factor correcting controller is adapted operatively to regulate the voltage across the load to a predetermined value. 15
18. Apparatus according to any preceding claim, wherein the voltage source comprises an AC source, the apparatus further comprising a rectifier, preferably a full wave rectifier, for rectifying the AC source. 20
19. Apparatus according to Claim 18, further characterized in that the rectified power from the input power source is operatively delivered via said short circuit path directly to the input of the boost conversion elements. 25
20. Apparatus according to any of Claims 1 to 17, characterized in further comprising separate full wave rectifier circuits, the first rectifier circuit being arranged operatively to be interposed between the input source and the boost conversion elements, and the second rectifier circuit being arranged operatively to be interposed between the input source and the additional conversion elements. 30 35
21. Apparatus according to Claim 20, further characterized in that the output of the second rectifier circuit is connected by a short circuit path to the input of the additional conversion elements. 40
22. Apparatus according to Claim 20, further characterized in that the rectifier circuits comprise six unidirectional elements forming two bridges each having four of the unidirectional elements, two of the unidirectional elements belonging to both bridges, one of the bridges having its output connected to the boost conversion elements, the other having its output connected to the additional conversion elements. 45 50
23. Apparatus according to any preceding claim, further characterized in that the additional conversion elements comprise a pair of converters adapted to operate in a power sharing arrange-

ment, preferably comprising power sharing control circuitry.

24. Apparatus according to Claim 23, characterized in further comprising reconfiguration control circuitry adapted for connecting the pair of converters either in series or in parallel.
25. Apparatus according to Claims 23 or 24, further characterized in that the reconfiguration control circuitry is arranged to connect the pair of converters in series when the voltage of the input source crosses a threshold.
26. Apparatus according to Claims 23, 24 or 25, further characterized in that the reconfiguration control circuitry is arranged to connect the pair of converters in parallel when the voltage of the input source crosses a threshold.
27. Apparatus according to Claims 25 or 26, further characterized in that the threshold is related to the maximum input operating voltage of either converter.
28. Apparatus according to any of Claims 23 to 27, further characterized in that the converters are adapted operatively to share essentially equally in the power delivered to the load.
29. Apparatus according to any of Claims 23 to 28, further characterized in that the converters comprise ZCS converters, preferably one comprising a booster and the other comprising a driver.
30. Apparatus according to Claim 29, further characterized in that each of the converters of the pair has a positive input and a negative input, and further comprising a switch connecting the positive inputs of the two converters, a switch connecting the negative inputs of the two converters, and a diode connecting the positive input of one of the converters to the negative input of the other converter.
31. Apparatus according to any of Claims 1 to 22, further characterized in that the additional conversion elements comprise more than two converters adapted to operate in a power sharing arrangement.
32. Apparatus according to Claim 23, characterized in further comprising output control circuitry adapted to connect the outputs of the pair of converters either in series or in parallel.
33. Apparatus according to Claim 32, further characterized in that the output control circuitry is ar-

ranged to connect the outputs of the pair of converters in series when the voltage at the input of the converters crosses a threshold.

34. Apparatus according to Claims 32 or 33, further characterized in that the output control circuitry is arranged to connect the outputs of the pair of converters in parallel when the voltage at the input of the converters crosses a threshold. 5
35. Apparatus according to Claims 33 or 34, further characterized in that the threshold is related to the minimum input operating voltage of either converter. 10
36. A method for converting power from a varying voltage source and delivering it to a load, comprising causing selectively  
a boost conversion of power originating from the varying voltage source in boost conversion elements, and  
another conversion of power originating from the varying voltage source in additional conversion elements, 20  
in a manner, with respect to delivery of power to the load, to achieve greater conversion efficiency than if all of the power delivered to the load were constrained to flow through the additional conversion elements and at least some of the boost conversion elements. 25
37. A method according to Claim 36, wherein the conversions are caused selectively to achieve a greater input voltage operating range for the apparatus than if all of the power delivered to the load were constrained to flow only through the additional conversion elements. 30
38. A method according to Claims 36 or 37, further comprising power factor correcting the conversion of power. 35
39. A method according to any of Claims 36 to 38, wherein the additional conversion is caused to occur in two converters. 40
40. A method according to Claim 39, further comprising selectively connecting the inputs of the two converters in parallel or series. 45
41. A method according to Claim 39, further comprising selectively connecting the outputs of the two converters in parallel or series. 50
42. Apparatus for converting power from a voltage source having a predetermined source voltage range, and delivering it to a load, characterized in comprising: two sets of power conversion ele-

ments, each set being adapted for effecting conversion of power from the voltage source, at least one of the sets having an input operating voltage range narrower than the source voltage range; and control circuitry adapted for operatively configuring and reconfiguring interconnections of the two sets with the voltage source and the load to provide an input operating voltage range for said apparatus which is greater than the input operating range of the set of power conversion elements having the narrower input operating voltage range.

43. Apparatus according to Claim 42, further characterized in that the two sets are adapted to operate in a power sharing arrangement. 15
44. Apparatus according to Claim 43, further characterized in that the sets share essentially equally in the power delivered to the load. 20
45. Apparatus according to any of Claims 42, 43 or 44, further characterized in that the control circuitry is adapted operatively to connect the outputs of the two sets either in series or in parallel. 25
46. Apparatus according to Claims 42 to 45, further characterized in that the control circuitry is arranged to connect the outputs of the two sets in series when the voltage at the input of the two sets crosses a threshold. 30
47. Apparatus according to any of Claims 42 to 46, further characterized in that the control circuitry is arranged to connect the outputs of the two sets in parallel when the voltage at the input of the two sets crosses a threshold. 35
48. Apparatus according to any of Claims 46 or 47, further characterized in that the threshold is related to the minimum input operating voltage of either of the sets. 40
49. Apparatus according to any of Claims 42 to 48, further characterized in that the two sets comprise ZCS converters. 45
50. A method for enhancing the input voltage operating range of a power conversion circuit which has two sets of power conversion elements arranged to share power delivered to a load, comprising  
selectively configuring the circuit with the two sets in series or not in series in a manner so that the input voltage operating range of the power conversion circuit is broader than the input voltage operating range of either of the sets of power conversion elements. 50

51. A method according to Claim 50, further comprising configuring the circuit with the two sets in parallel at times when they are not in series.
52. A method according to Claims 50 or 51, wherein the two sets are configured in series by configuring their inputs in series. 5
53. A method according to Claims 50, 51 or 52, wherein the two sets are configured in series by configuring their outputs in series. 10
54. A method according to Claim 51, wherein the two sets are configured in parallel by configuring their inputs in parallel. 15
55. A method according to Claim 51, wherein the two sets are configured in parallel by configuring their outputs in parallel. 20

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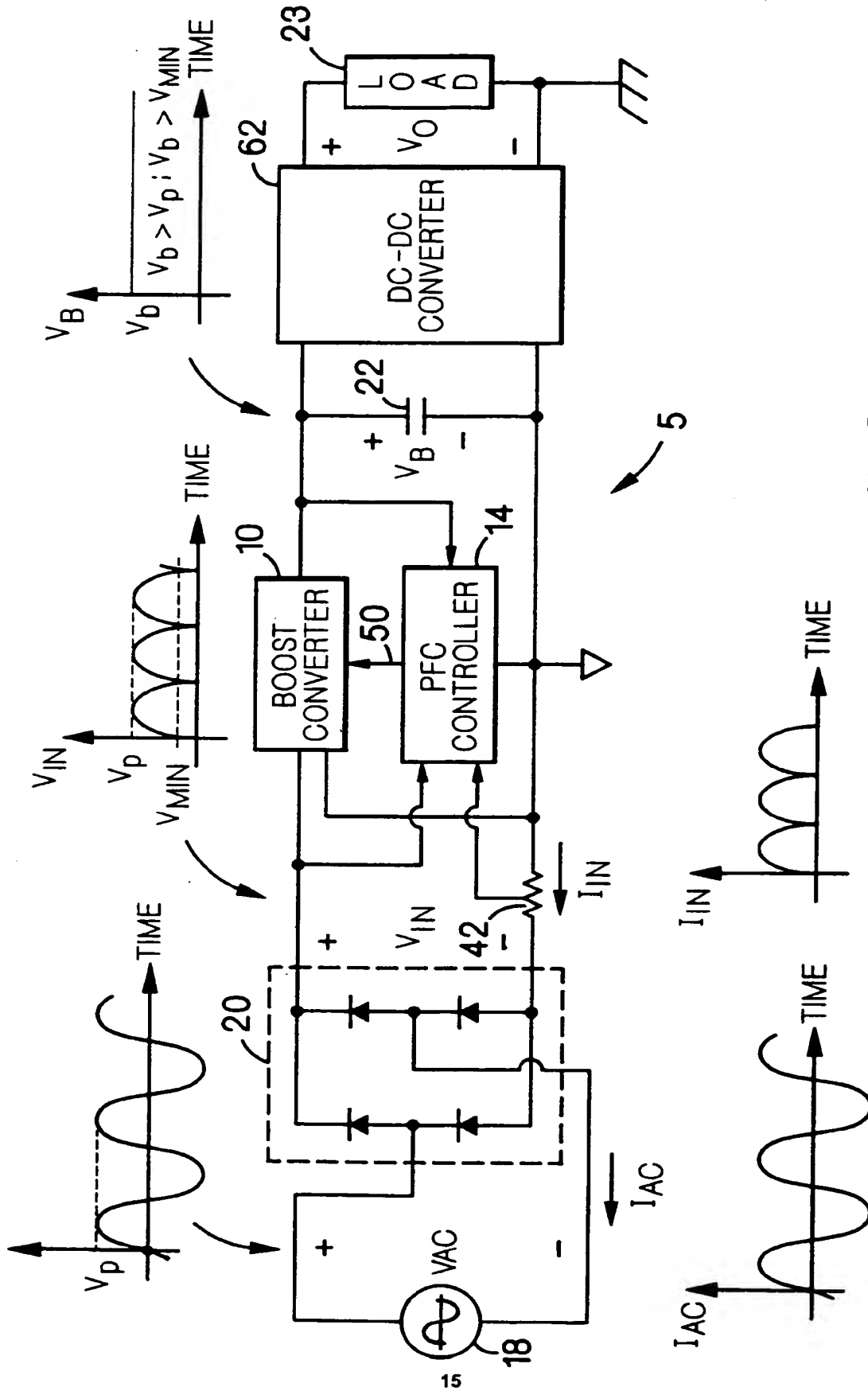
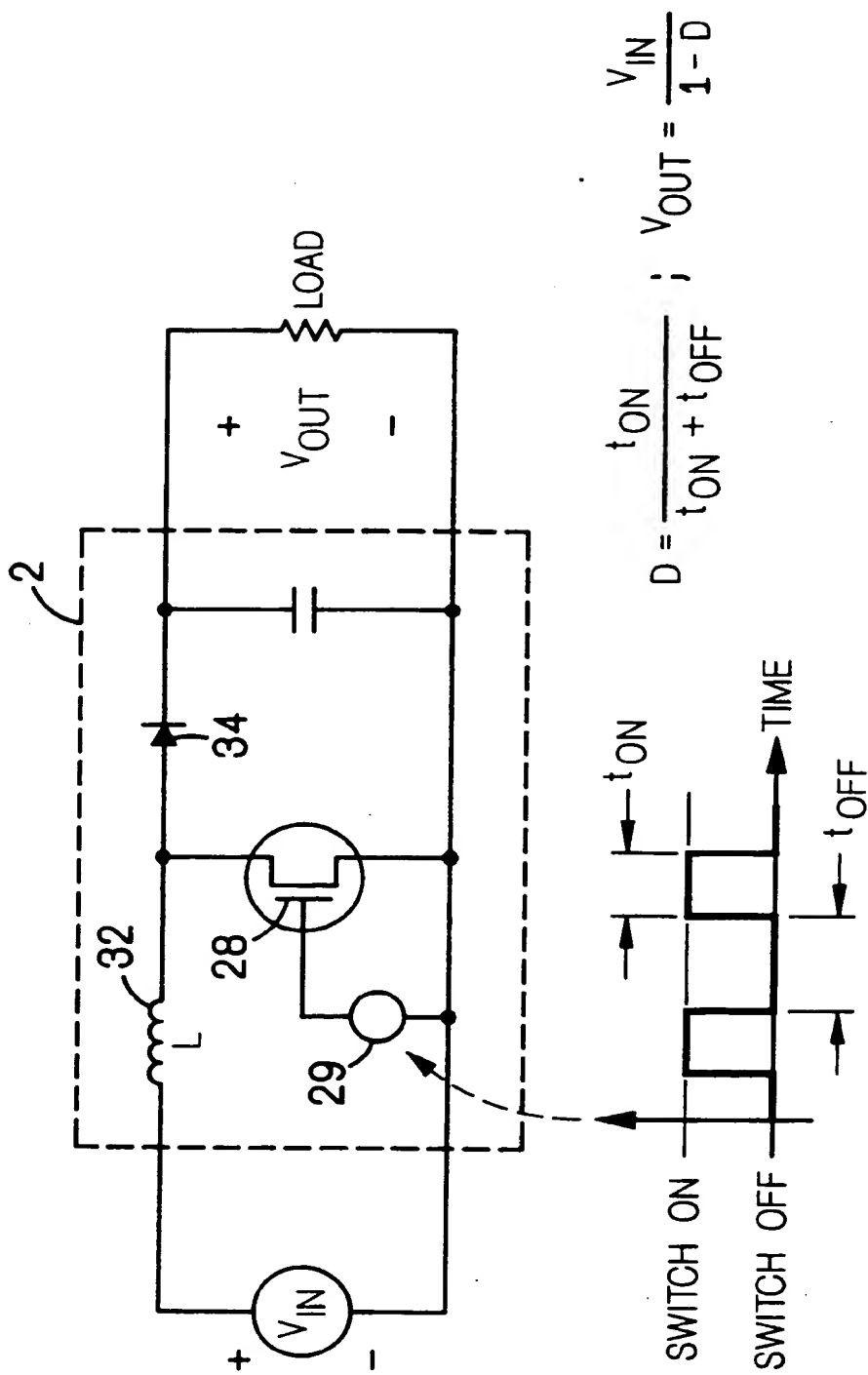


FIG.1

PRIOR ART





PRIOR ART

FIG. 2

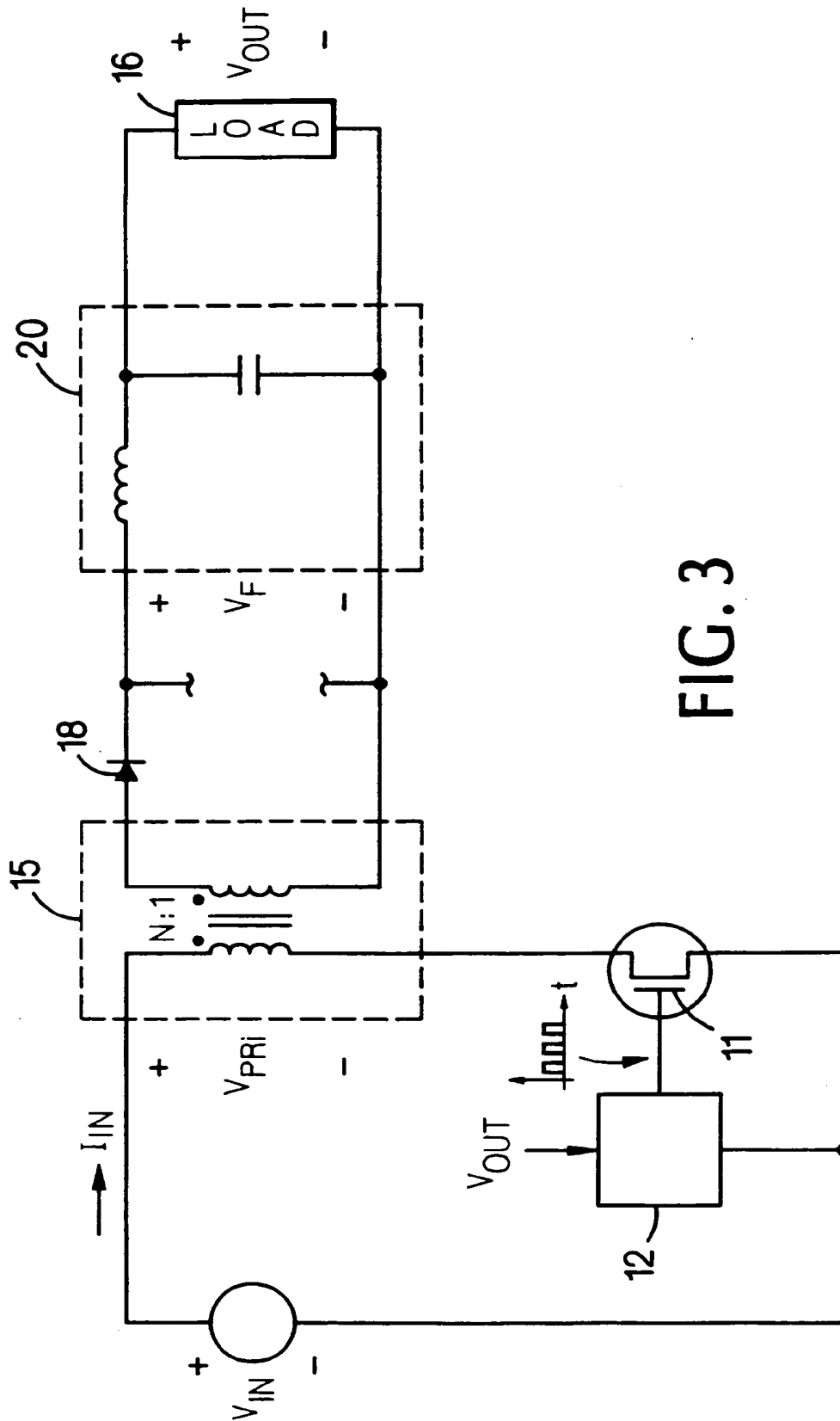


FIG. 3

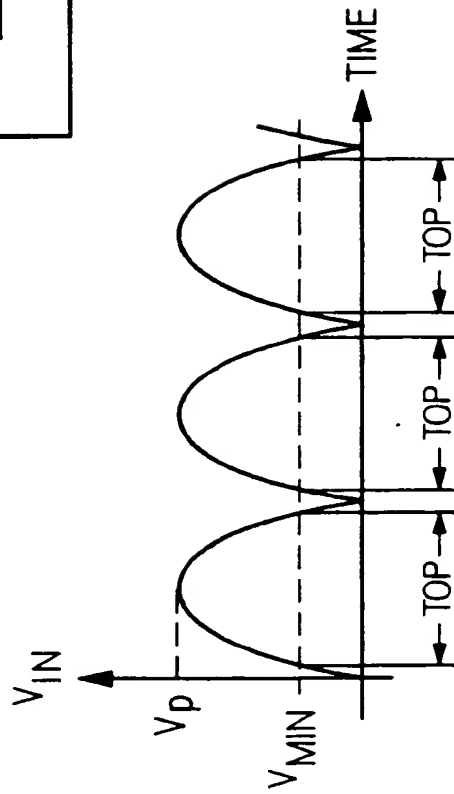
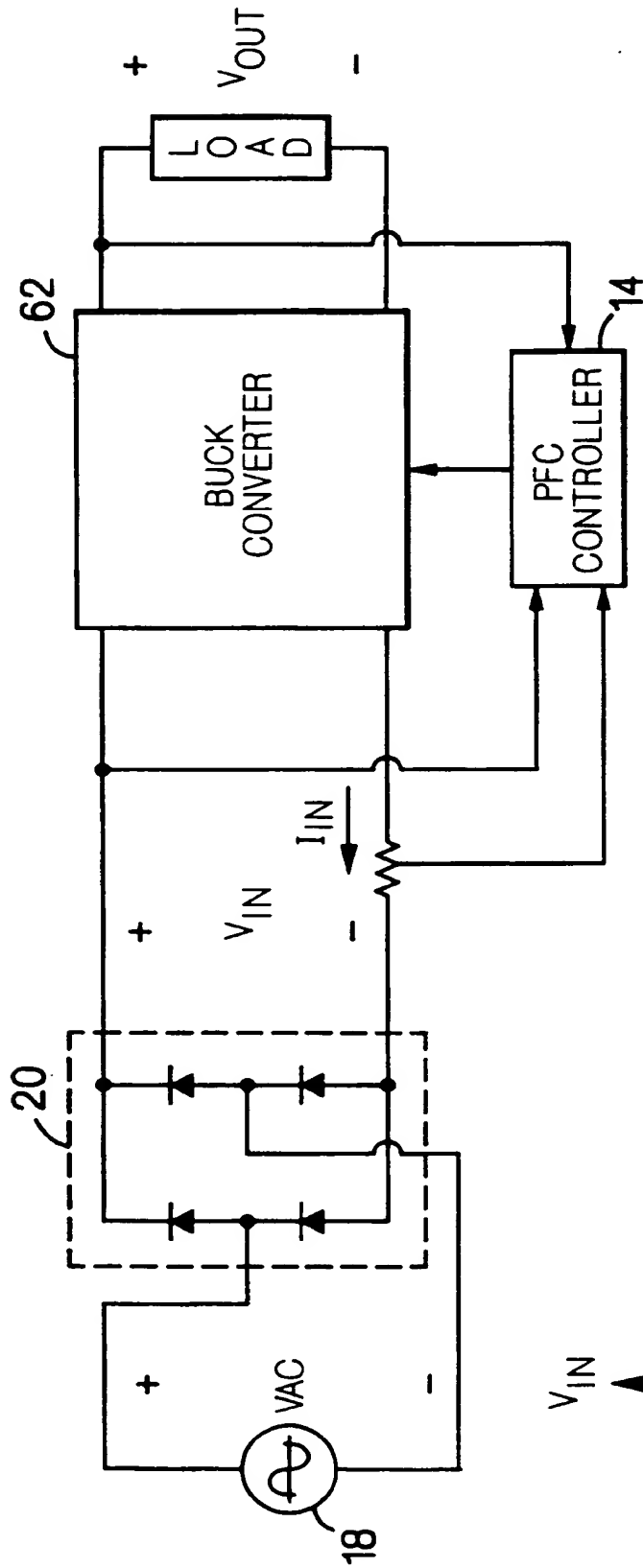


FIG. 4

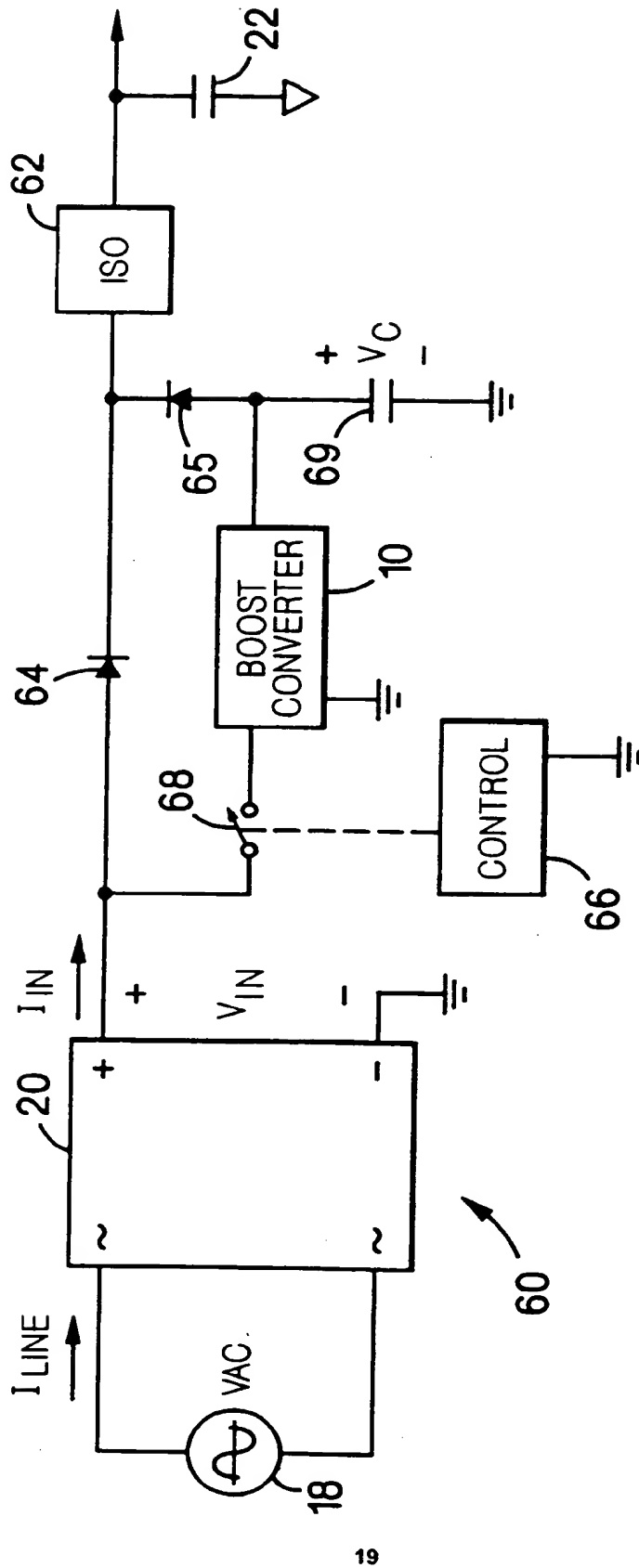


FIG. 5

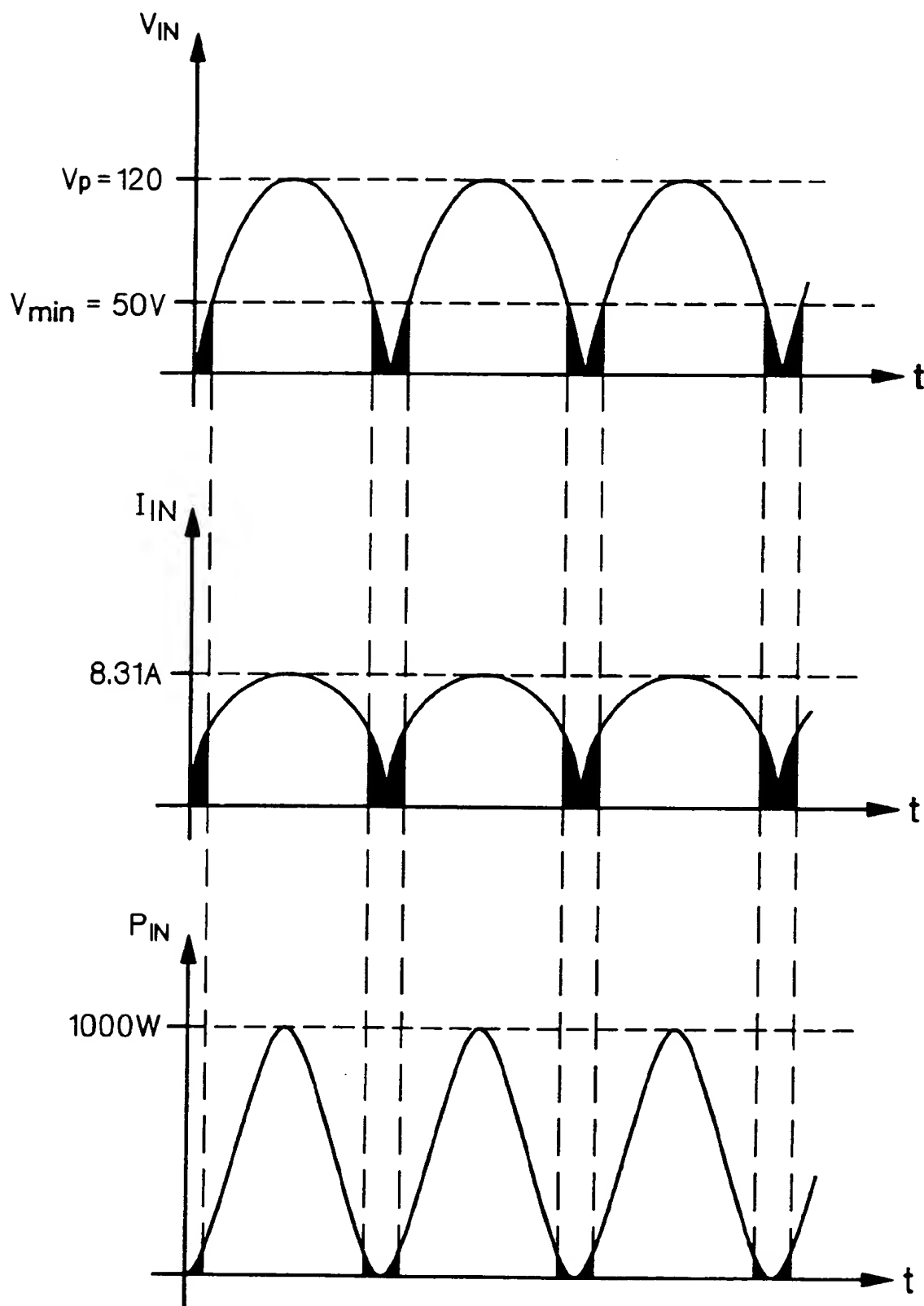


FIG. 6

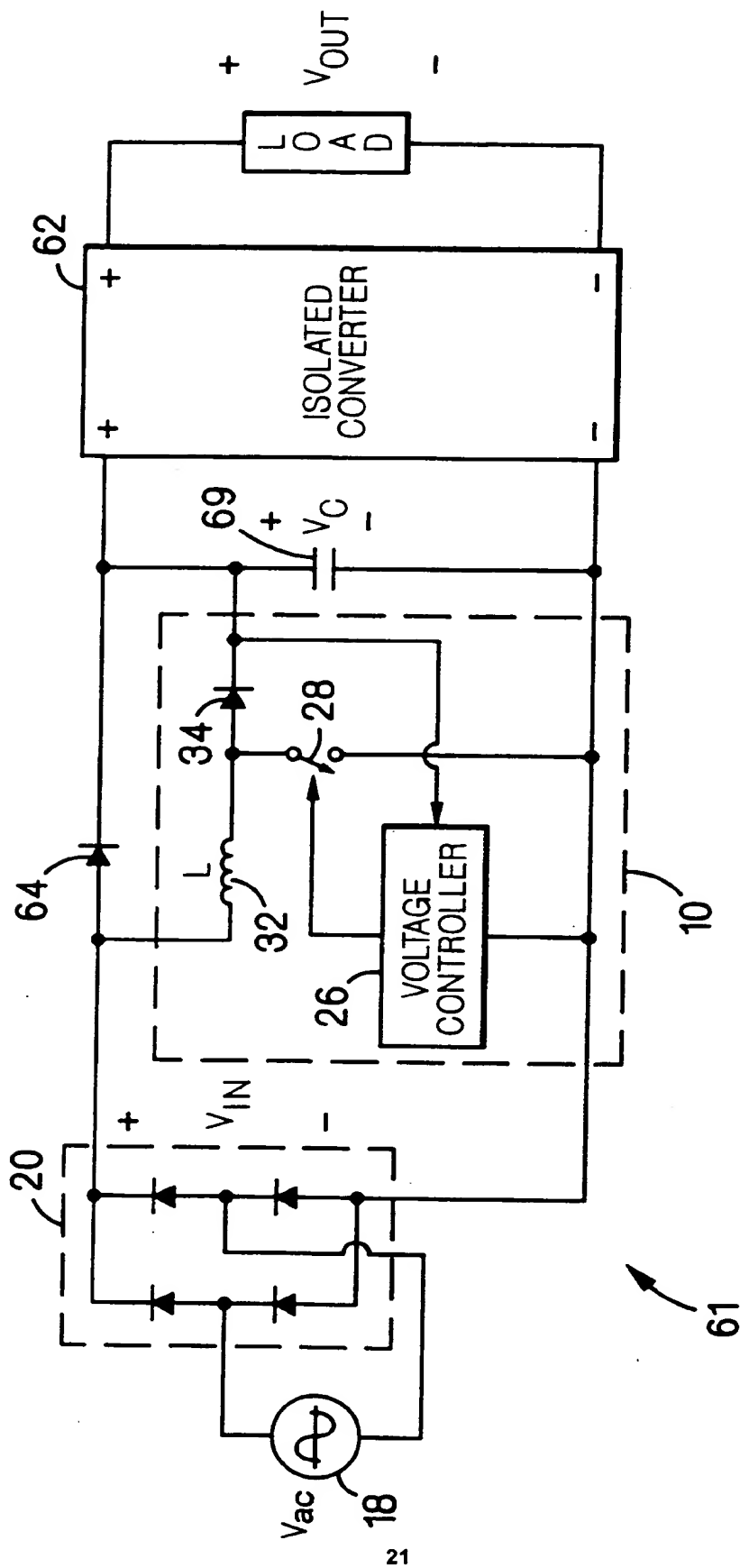
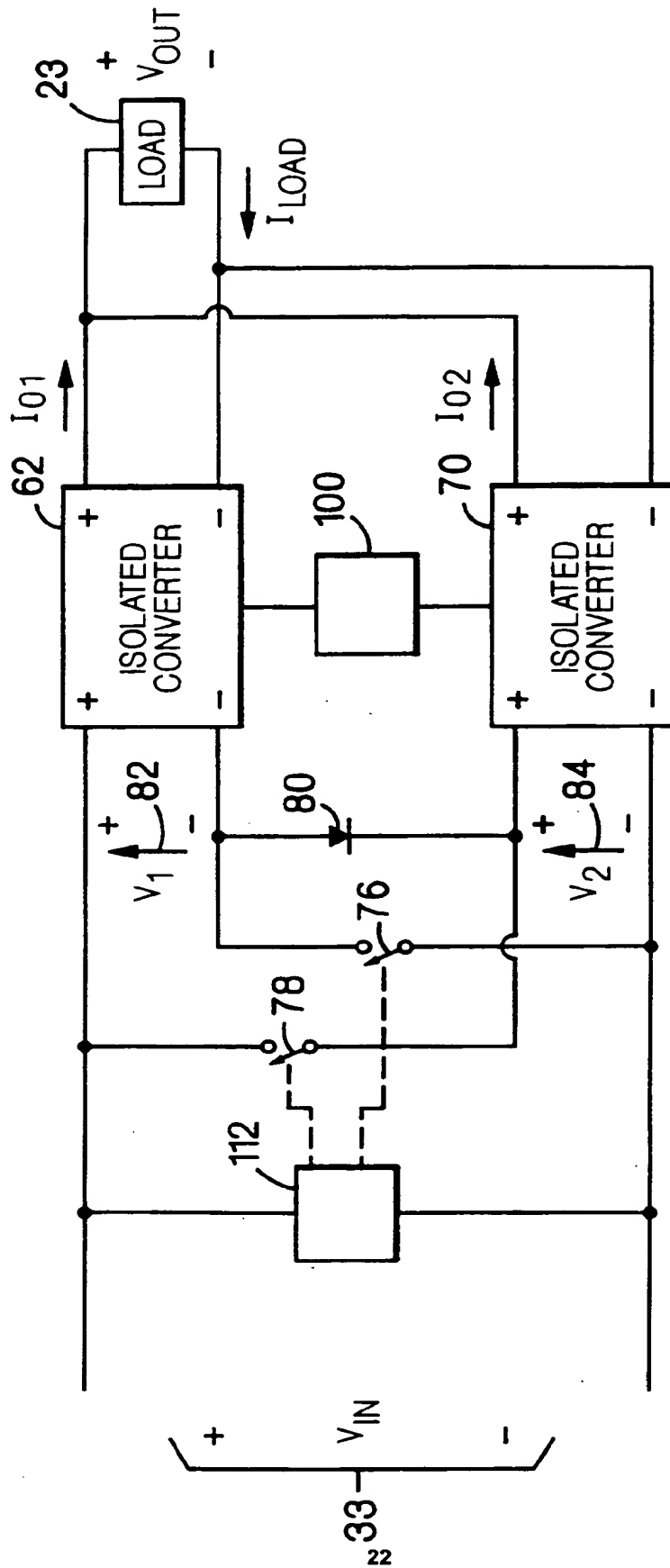


FIG. 7



8.  
G.  
F.



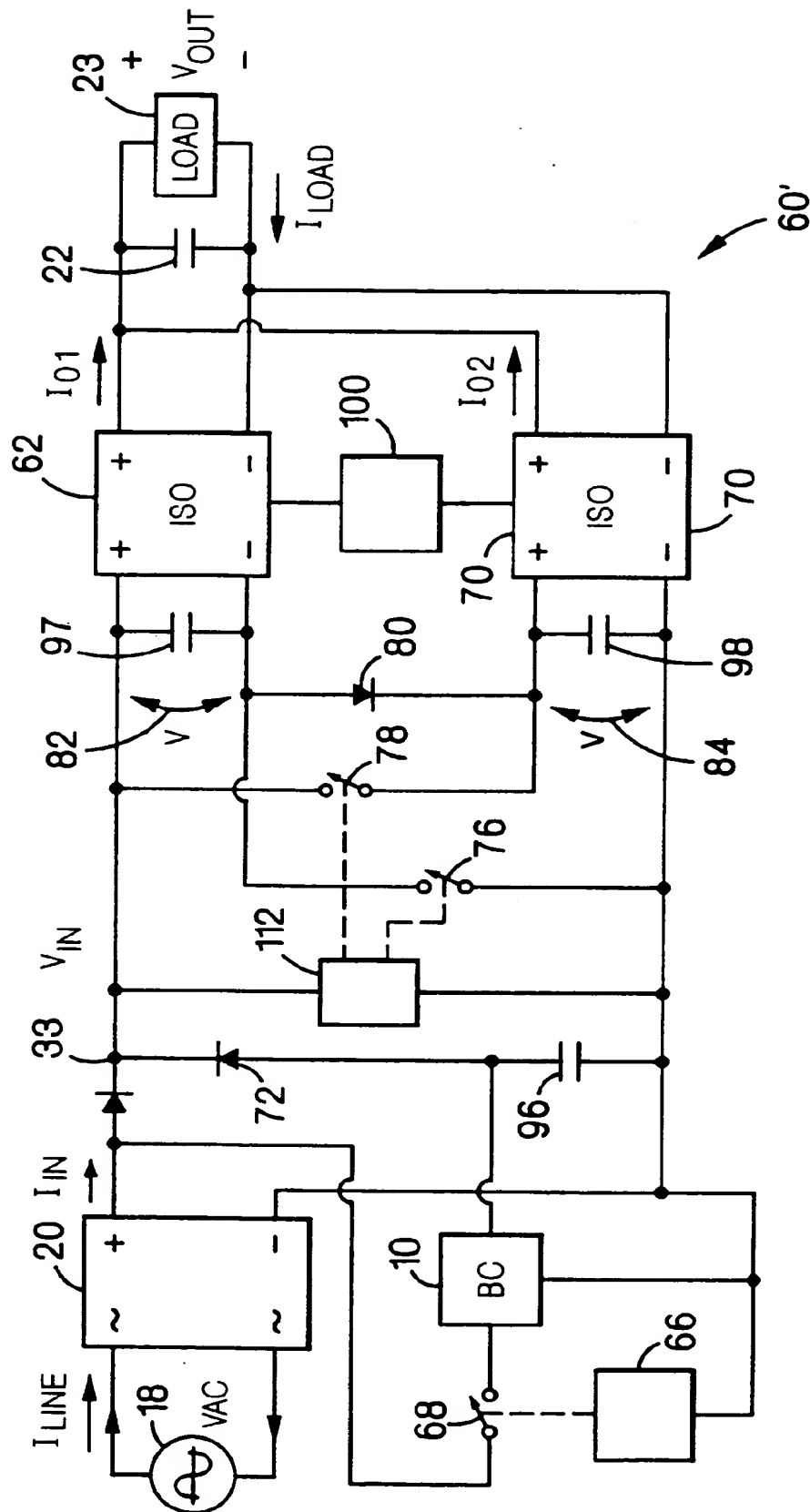


FIG. 9

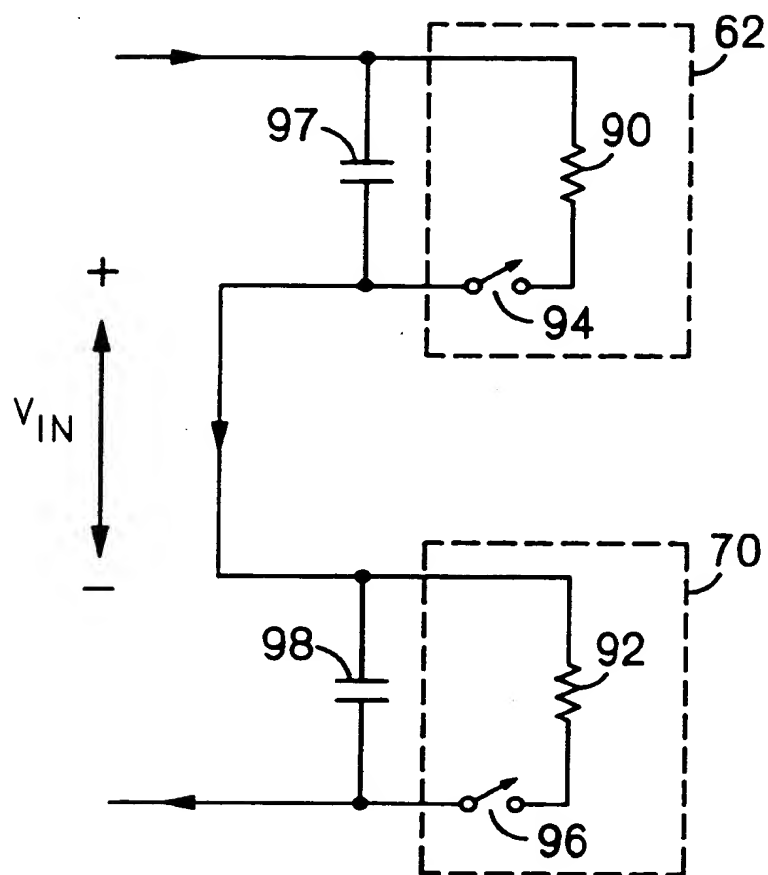


FIG. 10

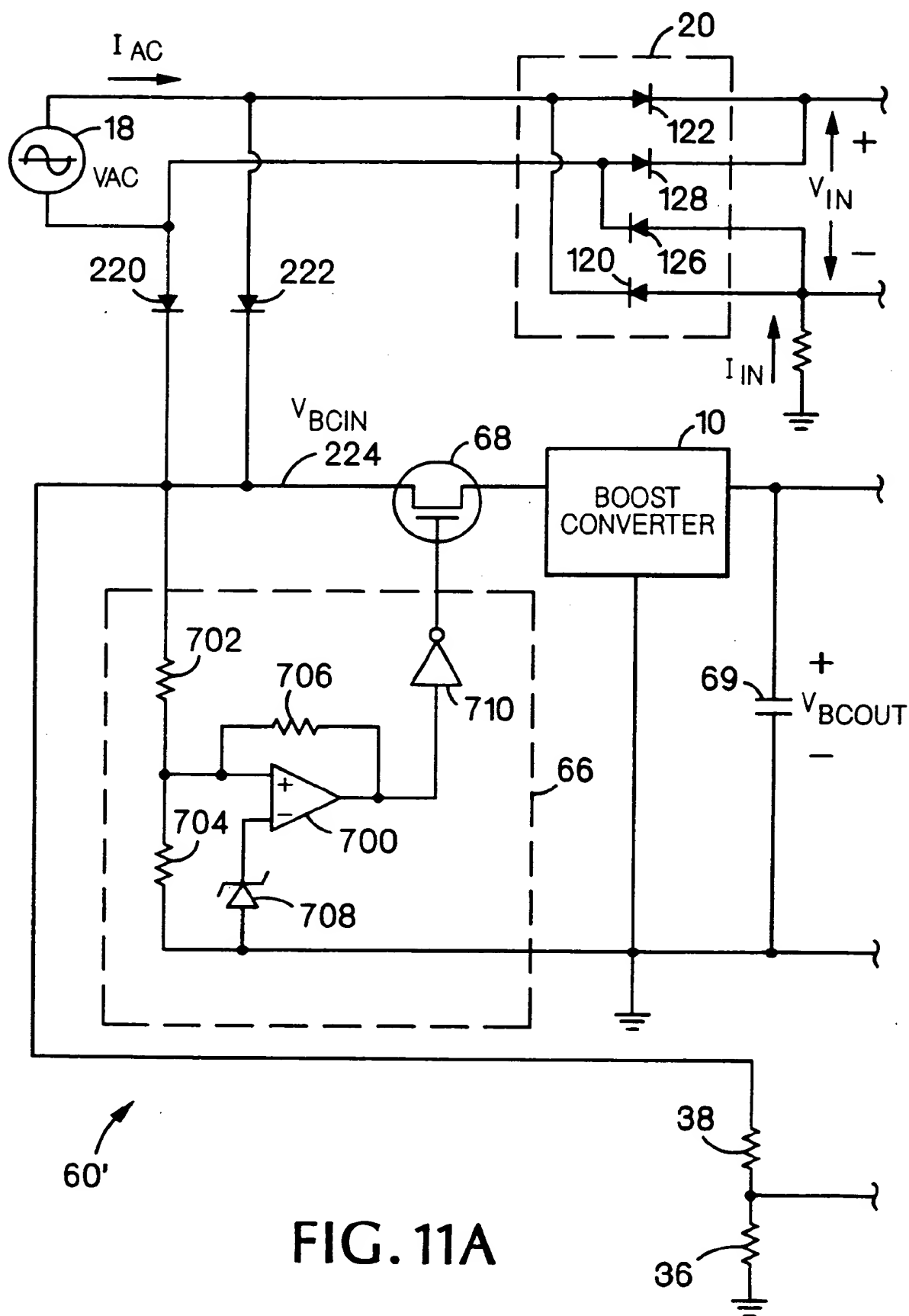


FIG. 11A

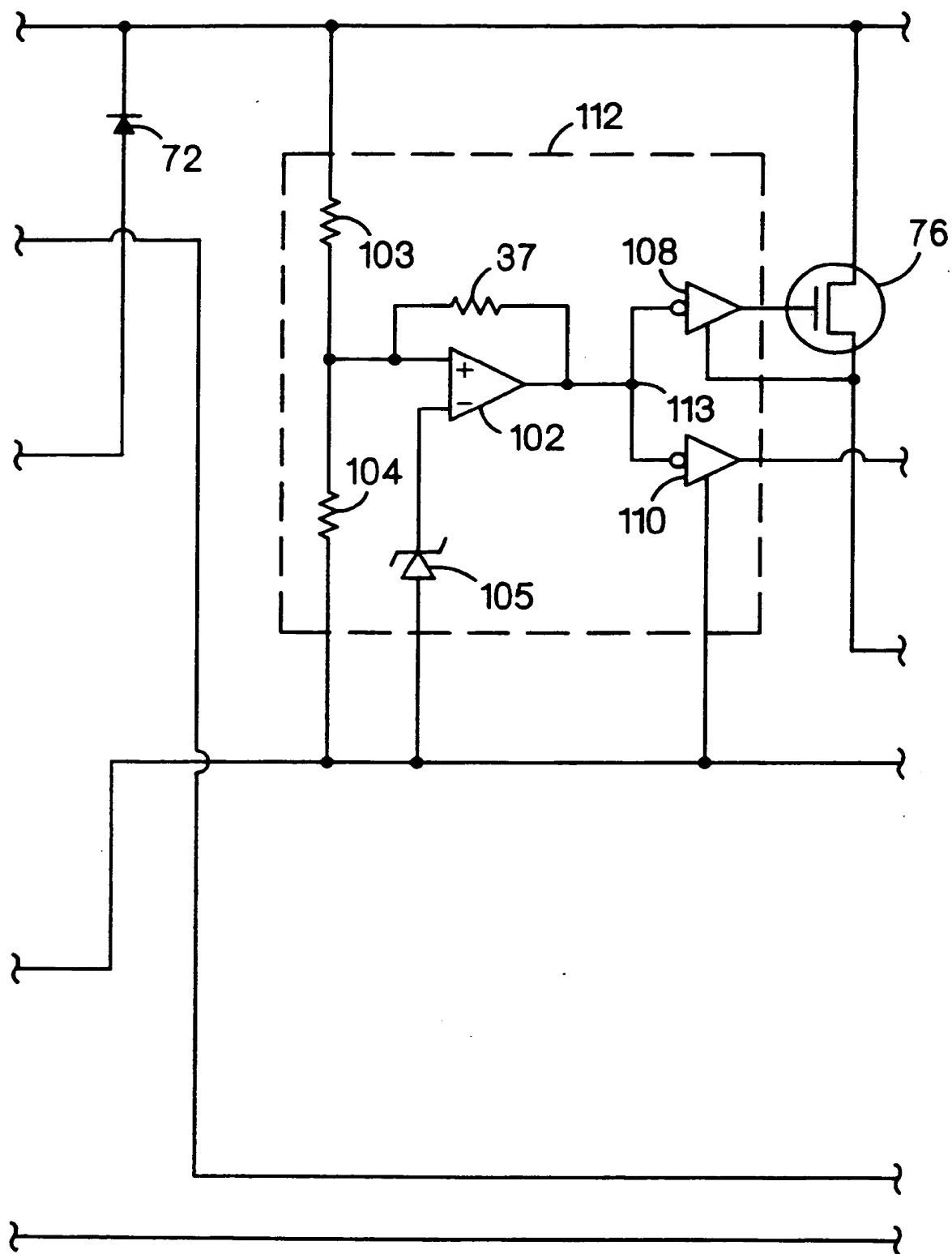
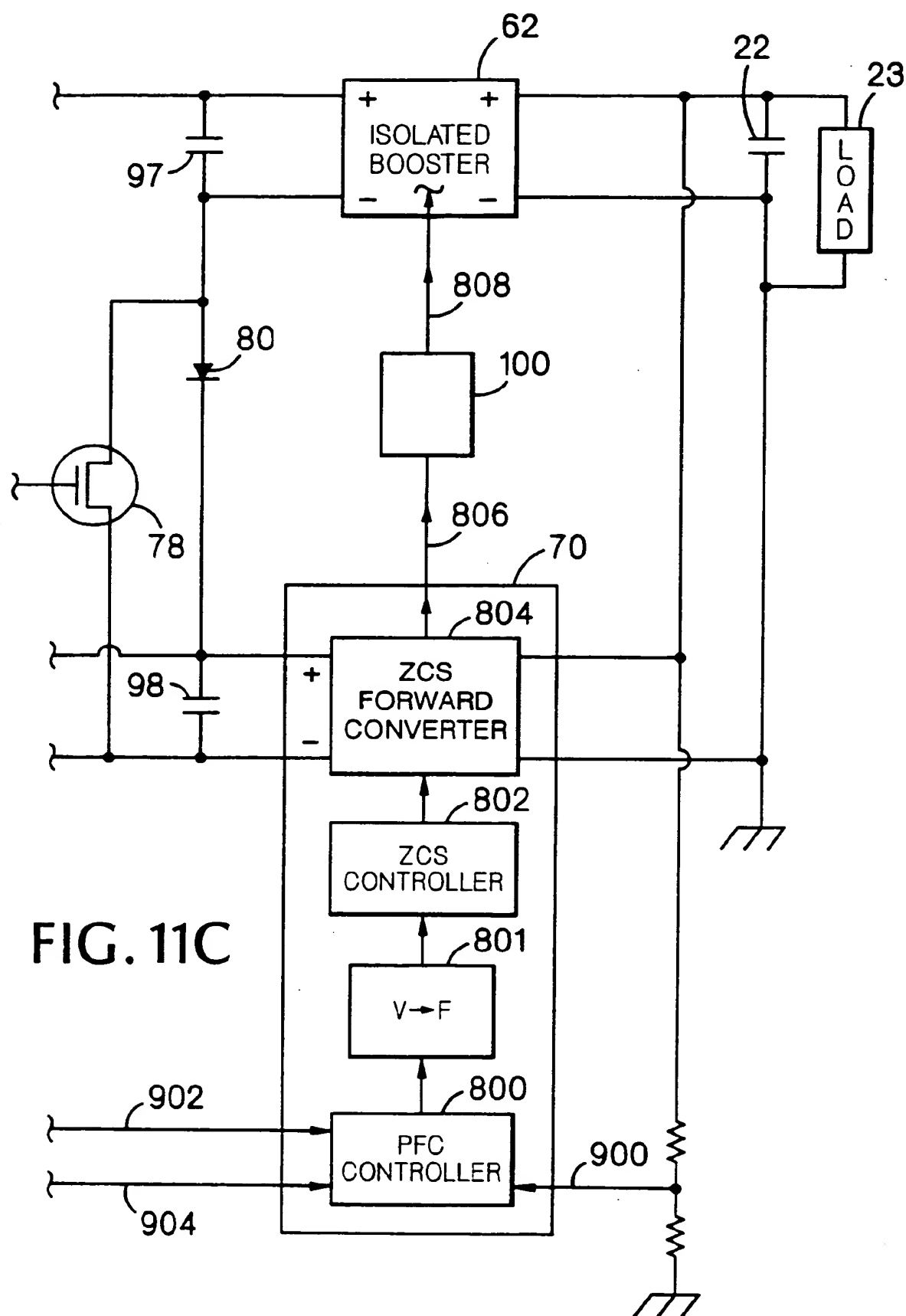
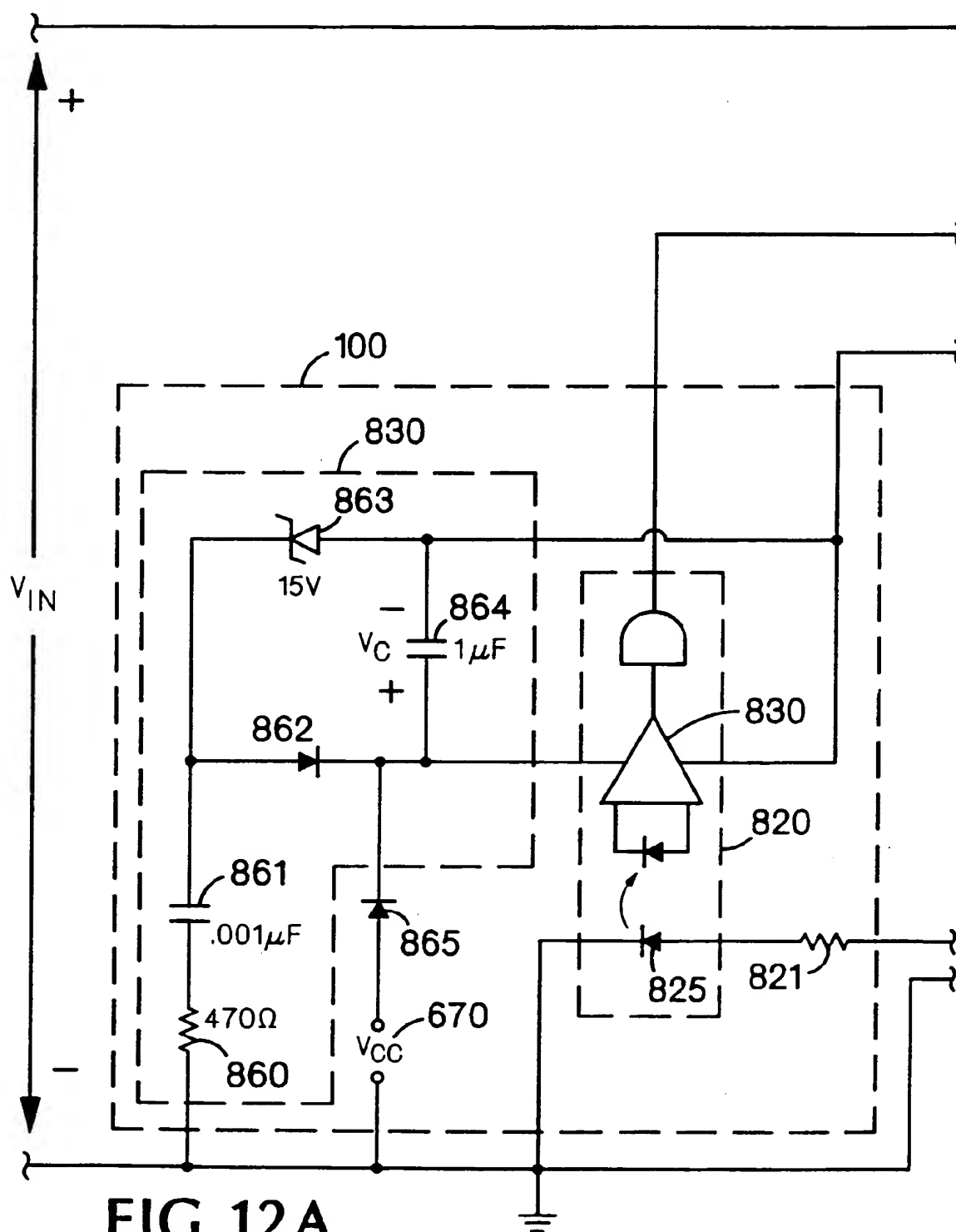


FIG. 11B





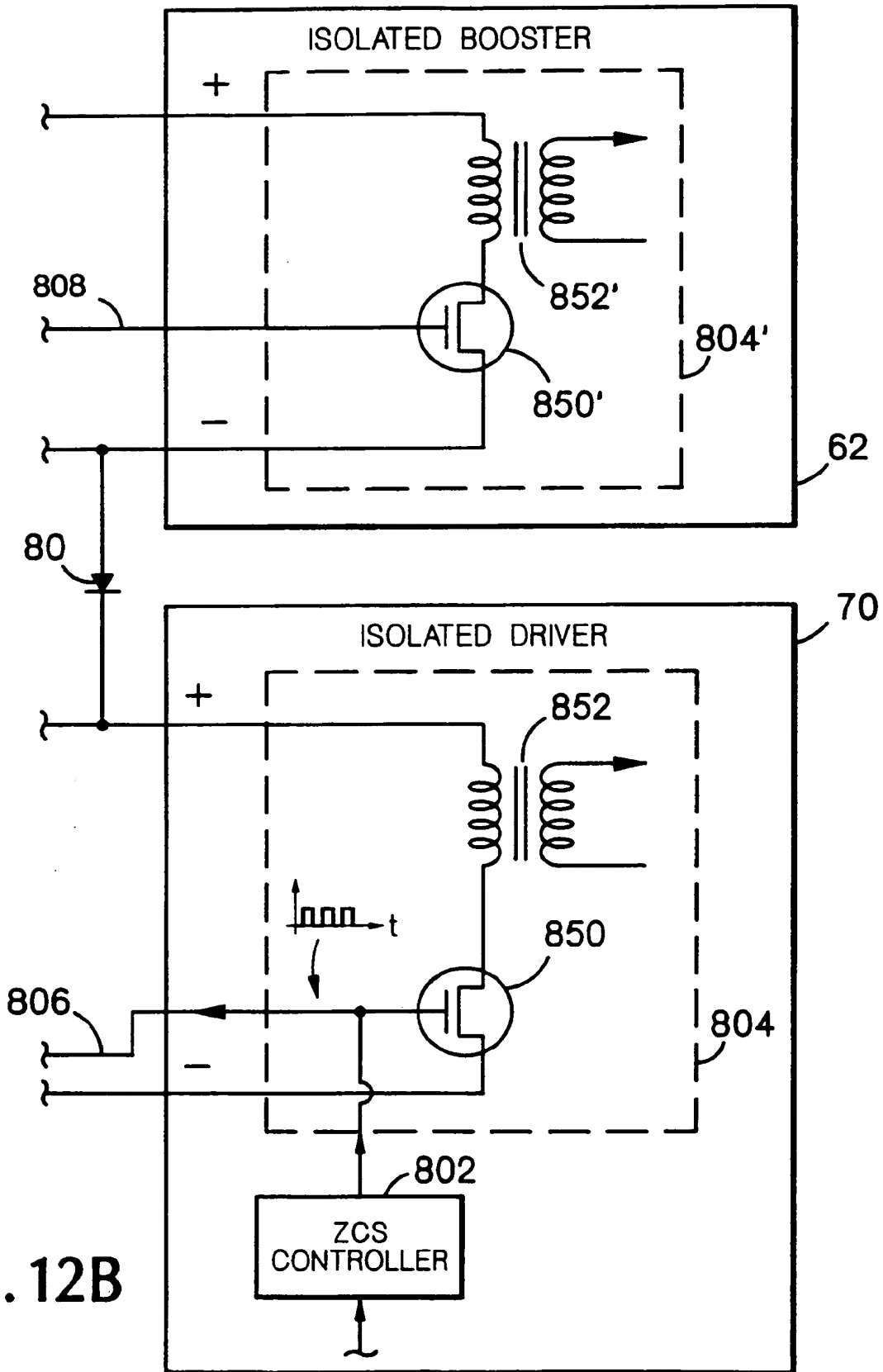
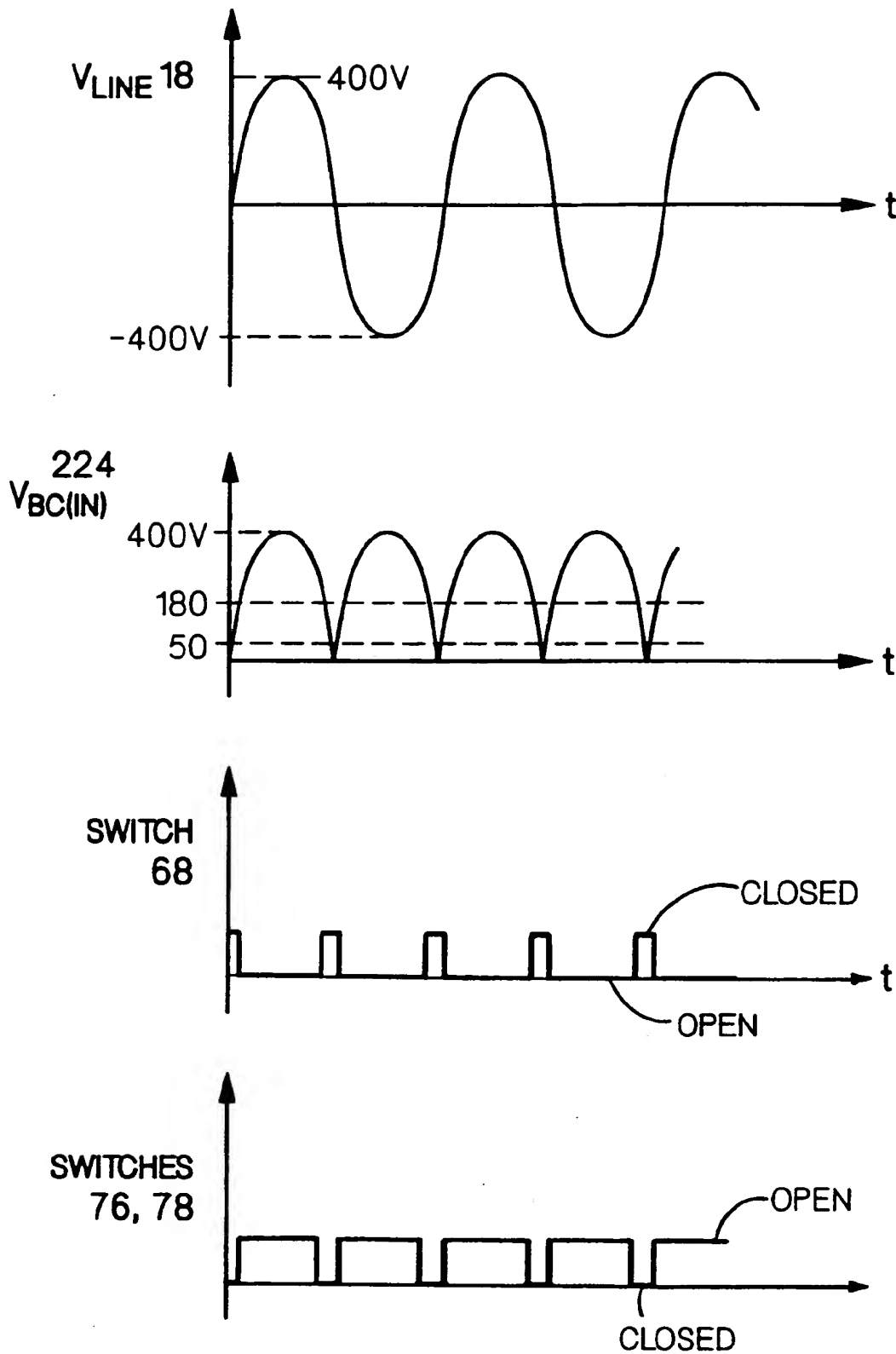


FIG. 12B





**FIG.13**

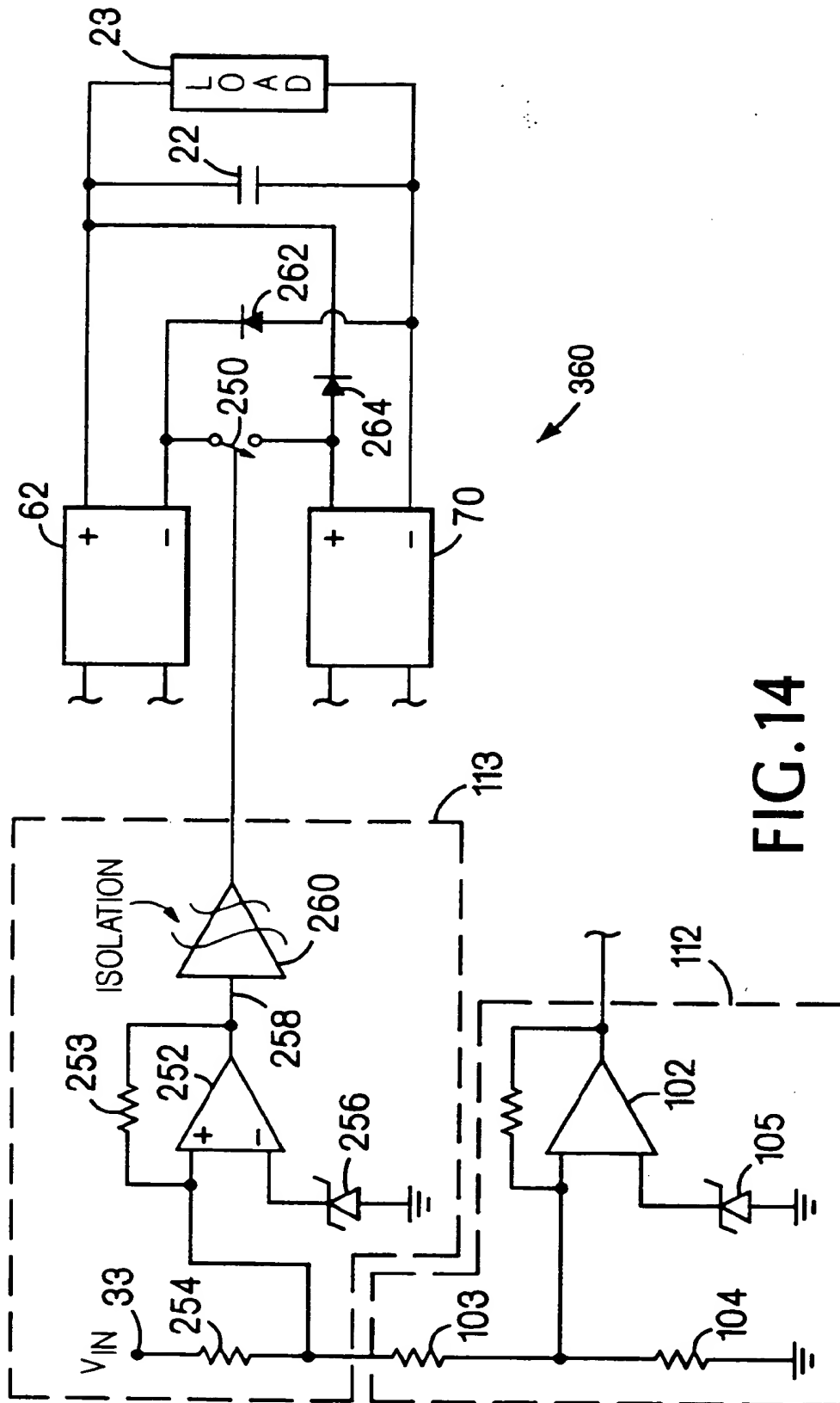
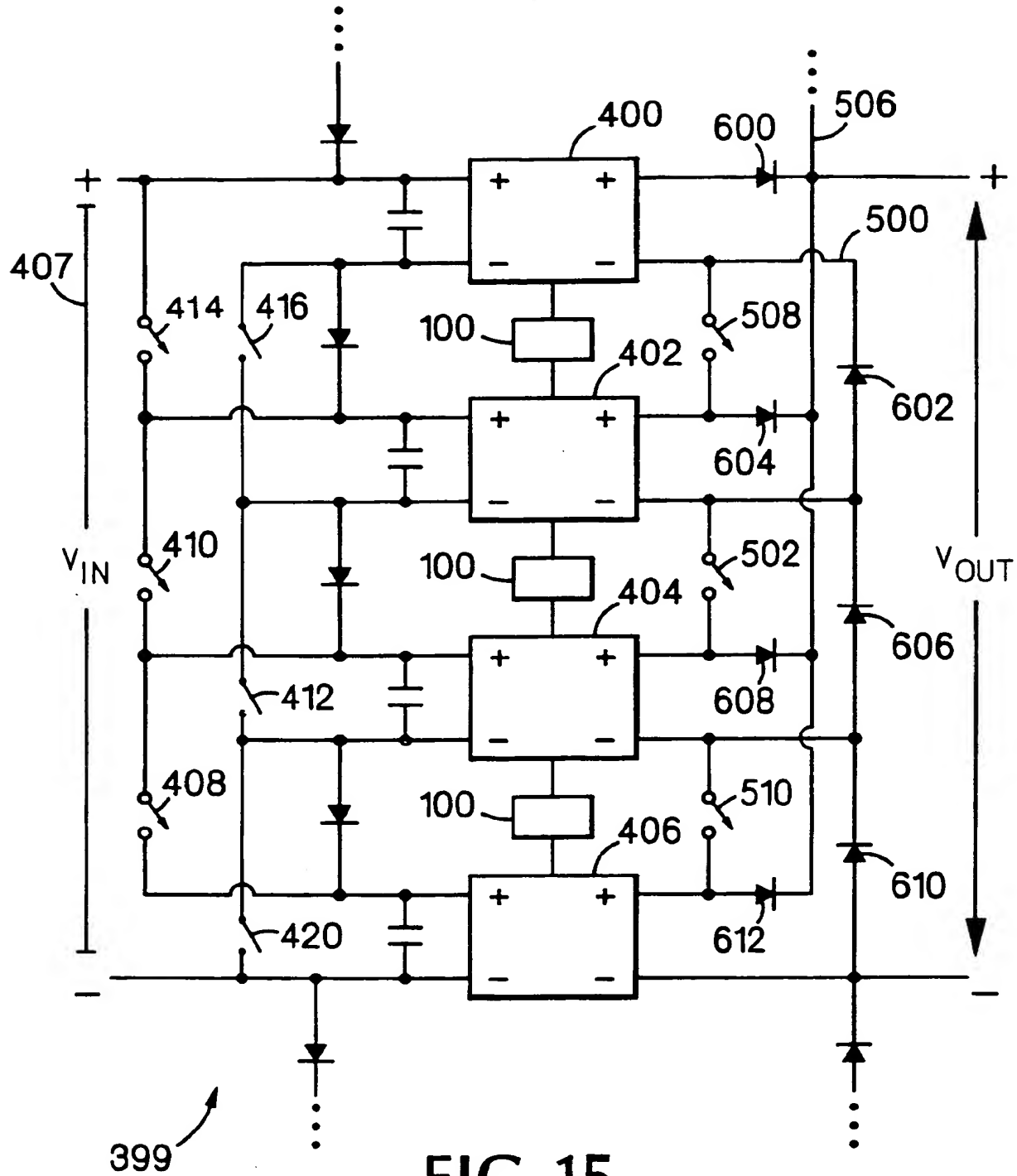
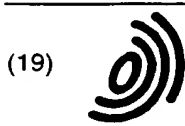


FIG. 14





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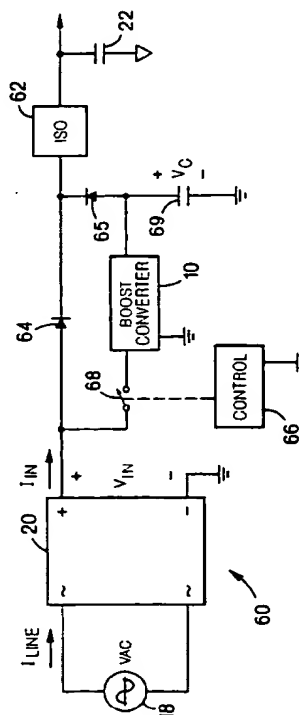
(54) Efficient power conversion

(57) A power conversion apparatus consisting of boost conversion elements for effecting a boost conversion of power originating from a varying voltage source and additional conversion elements for also effecting conversion of power originating from the varying voltage source is disclosed. Circuitry selectively configures the conversion elements with respect to delivery of power to a load to achieve greater conversion efficiency than if all of the power delivered to the load were constrained to flow through the additional conversion elements and at least some of the boost conversion elements.

Also disclosed is a power conversion scheme in which power is converted from a voltage source having a predetermined source voltage range, and delivered to a load via two sets of power conversion elements. Each set effects conversion of power from the voltage source. At least one of the sets has an input operating voltage range narrower than the source voltage range. The apparatus includes control circuitry for configuring and reconfiguring interconnections of the two sets with the voltage source and the load to provide an input operating voltage range for the apparatus which is greater than the input operating range of the set of power conversion elements having the narrower input operating voltage range.

A way of enhancing the input voltage operating range for a power conversion circuit which has two sets of power conversion elements arranged to share power delivered to a load is also described. The circuit is selectively configured with the two sets in series or not in

series in a manner so that the input voltage operating range of the power conversion circuit is broader than the input voltage operating range of either of the sets of power conversion elements.





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# EUROPEAN SEARCH REPORT

Application Number  
EP 95 30 2329

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X	PATENT ABSTRACTS OF JAPAN vol. 17, no. 383 (E-1400), 19 July 1993 & JP-A-05 064432 (TOKYO ELECTRIC), 12 March 1993, * abstract * -----	1-10, 13-15, 18,19, 36,37	H02M1/12 H02M7/217 H02M3/158
			TECHNICAL FIELDS SEARCHED (Int.Cl.6)
			H02M
<del>Disputes concerning the patent have been drawn up for all claims</del>			
Place of search		Date of completion of the search	Examiner
THE HAGUE		23 April 1996	GENTILI, L
CATEGORY OF CITED DOCUMENTS X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document			

EP0 FORM 1503 01.92 (PM/C01)



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### CLAIMS INCURRING FEES

The present European patent application comprised at the time of filing more than ten claims.

- ☐ All claims fees have been paid within the prescribed time limit. The present European search report has been drawn up for all claims.
- ☐ Only part of the claims fees have been paid within the prescribed time limit. The present European search report has been drawn up for the first ten claims and for those claims for which claims fees have been paid, namely claims:
- ☐ No claims fees have been paid within the prescribed time limit. The present European search report has been drawn up for the first ten claims.

### LACK OF UNITY OF INVENTION

The Search Division considers that the present European patent application does not comply with the requirement of unity of invention and relates to several inventions or groups of inventions,

namely:

— see sheet B

- ☐ All further search fees have been paid within the fixed time limit. The present European search report has been drawn up for all claims.
- ☐ Only part of the further search fees have been paid within the fixed time limit. The present European search report has been drawn up for those parts of the European patent application which relate to the inventions in respect of which search fees have been paid, namely claims:
- ☒ None of the further search fees has been paid within the fixed time limit. The present European search report has been drawn up for those parts of the European patent application which relate to the invention first mentioned in the claims, namely claims: 1-41



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**LACK OF UNITY OF INVENTION**

The Search Division considers that the present European patent application does not comply with the requirement of unity of invention and relates to several inventions or groups of inventions, namely:

1. Claims 1-41 : Method and apparatus for power conversion, comprising boost conversion elements and additional conversion elements, wherein, during some periods, power flowing to the load is constrained not to flow through the boost conversion elements.
2. Claims 42-55 : Method and apparatus for power conversion comprising two sets of power conversion elements and control circuitry for configuring and reconfiguring interconnections of the two sets with the voltage source and the load.